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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 393 717 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 90107578.8

(51) Int. Cl.5: H03H 11/12

(22) Date of filing: 20.04.90

(30) Priority: 20.04.89 JP 100767/89
28.09.89 JP 252578/89
28.09.89 JP 252579/89

(43) Date of publication of application:
24.10.90 Bulletin 90/43

(84) Designated Contracting States:
DE ES FR GB IT

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(54) Active filter circuit.

(57) An active filter circuit includes a first and second differential pairs each having a pair of transistors. A capacitor is connected to a collector of each on transistor of the first and second differential pairs. A first and second negative feed-back paths are connected, respectively, between the collector and a base of one transistor of the first differential pair and between the collector of one transistor of the second differential pair and a base of the other transistor of the first differential pair. By applying suitable voltages to respective inputs of the differential pairs, the active filter circuit functions as a band-pass filter, lowpass filter, high-pass filter, band elimination filter or phase-shifting filter with the same circuit configuration. A current mirror circuit correlatively changes current amounts of the first and second differential pairs in response to a control voltage, whereby a filter characteristic can be changed.

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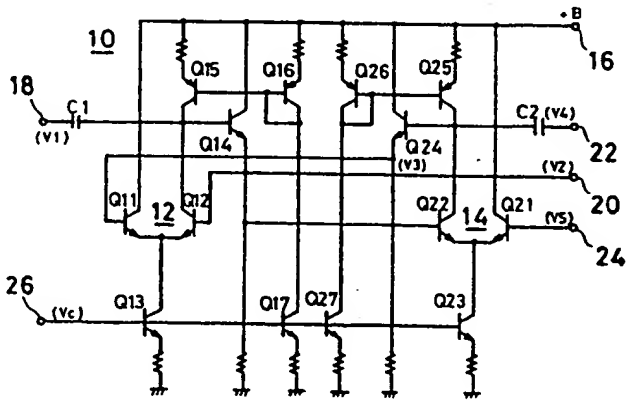


EP 0 393 717 A2

Active Filter Circuit

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an active filter circuit. More specifically, the present invention relates to an active filter circuit suitable for an integration circuit (IC).

Description of the Prior Art

In a case where a filter is to be incorporated in an integrated circuit, due to variations of elements in the IC, a fluctuation takes place in a filter characteristic. Conventionally, in order to compensate such a fluctuation, there was one method in which a dummy reference filter is provided in the IC and a reference signal is inputted thereto, and a feed-back control is applied to the reference filter so that a value of an output of the reference filter becomes a desired value. Based upon an idea that since a filter to be controlled comprises resistors and capacitors being the same as or correlative to that of the reference filter and therefore, a filter characteristic of the filter to be controlled can be adjusted to the same as or correlative to the characteristic of the reference filter if and when the same or correlative control signal is applied thereto, this method is a method for controlling the other filter to be controlled within the IC.

A prior art shown in Fig. 1 is one example of a case where a cut-off frequency fc of a lowpass filter is automatically controlled. First, a reference signal having a predetermined reference frequency Fref is inputted to a reference filter, and a level of a signal that is obtained by amplifying an output of the reference filter is compared with an output level of a reference frequency signal oscillator, a control voltage Vc by which both the levels are become coincident with each other is outputted, and the control voltage is applied to a variable capacitance diode Cv so that the filter characteristic is changed. By applying this feed-back control, when an attenuation amount at the reference frequency in the filter becomes equal to a gain of the amplifier, both the levels becomes equal to each other and thus the filter is brought in an adjusted state.

In the conventional method shown in Fig. 1, it is not necessary to apply a signal from the external to adjust the filter incorporated in the IC; however, since a dummy reference filter is to be provided in the IC, not only the number of elements in the IC increases but also the reference signal oscillator is needed.

One example of a filter circuit suitable for an IC is disclosed in, for example, Japanese Patent Publication No. 61-55860 published on November 29, 1986.

In a filter circuit disclosed in Japanese Patent Publication No. 61-55806, in order to implement a high-pass filter circuit, it is necessary to add a subtracter, and therefore, there was a problem that not only the number of circuit components increases but also a circuit configuration becomes complex.

SUMMARY OF THE INVENTION

Therefore, a principal object of the present invention is to provide a novel active filter circuit.

Another object of the present invention is to provide an active filter circuit having a simple circuit configuration and suitable for an IC.

The other object of the present invention is to provide a various kind of filter controlling circuits which utilize such a novel active filter circuit.

An active filter circuit in accordance with the present invention comprises: a first differential pair constructed to include a first and second transistors; a first capacitive load connected to an output of the second transistor of the first differential pair; a first negative feed-back path for feeding-back an output of the second transistor to an input thereof; a second differential pair constructed to include a third and fourth transistors; a second capacitive load connected to an output of the fourth transistor of the second differential pair; and a second negative feed-back path for feeding-back an output of the fourth transistor to an input of the first transistor constituting the first differential pair.

In this invention, by the first and second negative feed-back paths, both of the first and second

differential pairs become to operate in the vicinity of a center of a linear region thereof, and therefore, the first and second differential pairs cooperates to function as a secondary active filter circuit.

In another aspect, an active filter circuit in accordance with the present invention comprises: a first differential pair constructed to include a first and second transistors of first capacitive load connected to an output of the second transistor of the first differential pair; a second differential pair constructed to include a third and fourth transistors; a connecting path for connecting an output of the second transistor of the first differential pair to an input of the fourth transistor of the second differential pair; a second capacitive load connected to an output of the fourth transistor; and a negative feed-back path for feeding-back an output of the fourth transistor to an input of the first transistor constituting the first differential pair.

In this aspect, by the connecting path and the negative feed-back path, both of the first and second differential pairs become to operate in the vicinity of a center of a linear region thereof, and therefore, the first and second differential pairs cooperate to function as a secondary active filter circuit.

In accordance with the present invention, since it is not necessary to provide additional circuits such as a subtracter and etc., it is possible to obtain an active filter circuit suitable for an IC without the increase of the number of circuit components and the complication of the circuit configuration.

Furthermore, in accordance with the present invention, since different kind of filters can be constructed by the same circuit configuration, respective filters are very correlative with each other, and therefore, it is possible to adjust the filters very easy.

The objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the embodiments of the present invention when taken in conjunction with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing a conventional method for automatically controlling a cut-off frequency of a lowpass filter.

Fig. 2A to Fig. 2C are circuit diagrams showing differential pairs which can be utilized in the present invention.

Fig. 3 is a circuit diagram showing one embodiment in accordance with the present invention.

Fig. 4 is a circuit diagram showing Fig. 3 embodiment in detail.

Fig. 5 is a circuit diagram showing another embodiment in accordance with the present invention.

Fig. 6 is a circuit diagram showing Fig. 5 embodiment in detail.

Fig. 7 is a circuit diagram showing a modified example of Fig. 4 embodiment.

Fig. 8 is a circuit diagram showing a modified example of Fig. 7 embodiment.

Fig. 9 is a circuit diagram showing a further modified example of Fig. 4 embodiment.

Fig. 10 is a circuit diagram showing a modified example of Fig. 9 embodiment.

Fig. 11 is a circuit diagram showing a modified example of Fig. 6 embodiment.

Fig. 12 is a circuit diagram showing a modified example of Fig. 11 embodiment.

Fig. 13 is a circuit diagram showing a further modified example of Fig. 6 embodiment.

Fig. 14 is a circuit diagram showing a modified example of Fig. 13 embodiment.

Fig. 15A to Fig. 15D are circuit diagrams respectively showing other embodiments in accordance with the present invention.

Fig. 16A to Fig. 16D are circuit diagrams respectively showing embodiments shown in Fig. 15A to Fig. 15D in detail.

Fig. 17 is a block diagram showing an embodiment of a phase locked loop (PLL) which utilizes an active filter circuit in accordance with the present invention.

Fig. 18 and Fig. 19 are block diagrams respectively showing modified examples in each of which a crystal filter is added to Fig. 17 embodiment.

Fig. 20 is a block diagram showing a chroma circuit as another embodiment in accordance with the present invention.

Fig. 21 is a block diagram showing a quadrature detecting circuit as another embodiment in accordance with the present invention.

Fig. 22 is a block diagram showing a VIF and SIF circuit as another embodiment in accordance with the present invention.

Fig. 23 is a block diagram showing an FM circuit as the other embodiment in accordance with the present invention.

DETAIL DESCRIPTION OF THE PREFERRED EMBODIMENTS

Prior to a description of specific active filter circuits in accordance with the present invention, first, a differential pair which includes a pair of transistors and can be utilized such active filter circuits will be described.

In a differential pair 1 composed of transistors Q1 and Q2 as shown in Fig. 2A, assuming that a load resistor is RL, a collector voltage V0 of the transistor Q2 is represented by the following equation (1);

$$V0 = gm * RL * (V3 - V2) \quad (1)$$

where gm is a mutual conductance.

Assuming that a charge of an electron is q, Boltzmann's constant is k, a current is I1, and an absolute temperature is T, a relationship represented by the following equation (2) is established.

$$gm = \frac{q \cdot (2I1)}{4kT} = \frac{qI1}{2kT} \quad \cdots(2)$$

In addition, an emitter resistor, that is, differential resistor re of each of the transistors Q1 and Q2 constituting the differential pair 1 is given by the following equation (3).

$$re = \frac{kT}{qI1} = \frac{1}{2gm} \quad \cdots(3)$$

Therefore, the above equation (1) can be modified as the following equation (4).

$$V0 = \frac{1}{2re} \cdot RL \cdot (V3 - V2) \quad \cdots(4)$$

Next, as shown in Fig. 2B, if the load resistor RL is replaced with a constant current source having a current amount of I1 and a capacitor C which serves as a capacitive load is connected to a collector of the transistor Q2, since an impedence of the constant current source can be regarded as infinity and an impedence $1/j\omega C$ due to the capacitor C is corresponding to the load resistor RL, the equation (4) can be modified as the following equation (5).

$$V0 = \frac{1}{2re} \cdot \frac{1}{j\omega C} \cdot (V3 - V2) \quad \cdots(5)$$

Now, as shown in Fig. 2B, if a voltage source having an output voltage of V1 is further connected between the capacitor C and the ground, the following equation (6) is obtainable.

$$V0 = \frac{1}{2re} \cdot \frac{1}{j\omega C} \cdot (V3 - V2) + V1 \quad \cdots(6)$$

Next, as shown in Fig. 2C, when a emitter follower is constructed by a transistor Q3, and an emitter voltage of the transistor Q3 can be given by the following equation (7) because an input voltage and an output voltage are equal to each other in the emitter follower.

$$V2 = \frac{1}{2re} \cdot \frac{1}{j\omega C} \cdot (V3 - V2) + V1 \quad \cdots(7)$$

In the differential pair 1 as shown in Fig. 2B or 2C, a base input of the transistor Q1 serves as a plus (+) input and a base input of the transistor Q2 serves as a minus (-) input, and an output voltage is withdrawn from the collector of the transistor Q2. Therefore, in the example of Fig. 2C, the output voltage V0 is fed-back to the (-) input through the emitter follower Q3.

With reference to Fig. 3, an active filter circuit 10 of this embodiment utilizes two differential pairs 12 and 14 each having the same configuration as that of the differential pair 1 described in Fig. 2A to 2C. An output voltage V3 of a second differential pair 14 is applied to a (+) input of a first differential pair 12 (corresponding to the base input of the transistor Q1 in Fig. 2C), and an output voltage V2 of the first differential pair 12 is fed-back to a (-) input thereof (corresponding to the base input of the transistor Q2 in Fig. 2C). Voltages V1 and V4 are respectively applied to capacitive loads of the differential pairs 12 and 14, that is, capacitors C1 and C2. To a (+) input of the second differential pair 14 (corresponding to the base input of the transistor Q1 in Fig. 2B), a voltage V5 is applied, and the output voltage V2 of the first differential pair 12 is fed-back to a (-) input thereof (corresponding to the base input of the transistor Q2 in Fig. 2B).

The active filter circuit 10 shown in Fig. 3 is specifically shown in Fig. 4. With reference to Fig. 4. the active filter circuit 10 includes the first differential pair 12 constructed to include a first and second transistors Q11 and Q12, and the second differential pair 14 constructed to include a third and fourth transistors Q21 and Q22.

Emitters of the transistors Q11 and Q12 constituting the first differential pair 12 are commonly connected to a collector of a transistor Q13 constituting the above described constant current source. A collector of the transistor Q11 is supplied with a power source voltage (+B) from a terminal 16. A collector of the transistor Q12 is connected to a constant current source, that is, a collector of a transistor Q15 and a base of a transistor Q14 constituting the above described emitter follower of the first differential pair 12, which is also connected to a terminal 18 through the capacitor C1 constituting the capacitive load. To a base input of the transistor Q11 constituting the (+) input of the first differential pair 12 of Fig. 3, an output of a transistor Q24 constituting the above described emitter follower of the second differential pair 14 is connected, and a base input of the transistor Q12 constituting the (-) input is connected to the output of the transistor Q14, that is, a terminal 20. In addition, a current amount of the constant current source constructed by the transistor Q13 is set as 2I1 that is double a current amount I1 of the constant current source constructed by the transistor Q15.

Emitters of the transistors Q21 and Q22 constituting the second differential pair 14 are commonly connected to the above described constant current source constructed by a transistor Q23 which constitutes a current mirror circuit together with the previous transistor Q13. A collector of the transistor Q21 is applied with the power source voltage (+B) from the terminal 16. A collector of the transistor Q22 is connected to a constant current source constructed by a transistor Q25 and a base of a transistor Q24 as the emitter follower, which is also connected to a terminal 22 through the capacitor C2 that is the capacitive load. A base input of the transistor Q22 constituting the (-) input of the second differential pair 14 of Fig. 3 circuit is connected to the output of the first differential pair 12, that is, the terminal 20, and a base input of the transistor Q21 constituting the (+) input is connected to a terminal 24. In addition, as similar to the previously described first differential pair 12, in the second differential pair 14, a current amount of the constant current source constructed by the transistor Q25 is set as 2I2 that is double a current amount I2 of the constant current source constructed by the transistor Q25.

Transistors Q16 and Q26 are paired with each other, respective collectors of which are supplied with the power source voltage (+B) via suitable resistors. A collector of the transistor Q16 is connected to a base thereof and a constant current source constructed by a transistor Q17. Similarlily, a collector of the transistor Q26 is connected to a base thereof and a constant current source constructed by a transistor Q27.

In addition, the transistors Q13, Q23, Q17 and Q27 constituting the above described constant current sources are connected in parallel with each other to construct a current mirror circuit, and the bases thereof are commonly connected to a terminal 26. By applying a control voltage Vc to the terminal 26, cuurent amounts of the respective transistors are changed, whereby a filter characteristic of this active filter circuit 10 can be adjusted or controlled.

Now, it is assumed that voltages at the terminal 18, the output of the transistor Q14, that is, the terminal 20, the output of the transistor Q24, the terminal 22 and the terminal 24 are respectively set as V1, V2, V3, V4 and V5.

When the voltage V5 at the terminal 24 increases, a collector current of the transistor Q22 decreses, and a current of the transistor Q24 increases by that decreased amount, and therefore, the output voltage V3 of the transistor Q24 increases. When the voltage V3 increases, a collector current of the transistor Q12 decreases, and a current of the transistor Q14 increases by that decreased amount, and therefore, the voltage V2 at the terminal 20 increases. When the voltage V2 increases, the decrease of the collector currents of the transistors Q12 and Q22 are suppressed so that operations of the first and second differential pairs 12 and 14 become stable. Therefore, each of the first and second differential pairs 12 and 14 always operates in the vicinity of a center of a linear region thereof, and therefore, no distortion of the signals occurs and a good filter characteristic is obtainable.

In the active filter circuit 10 shown in Fig. 4, on the assumption that the emitter resistor of each of the transistors Q11 and Q12 is re1, a current I1 flowing each of the transistors Q11 and Q12 of the first differential pair 12 is given by the following equation (8).

$$I1 = \frac{V3 - V2}{2re1} \quad \cdots (8)$$

In addition, a signal voltage of the capacitor C1 is given by the following equation (9).

$$VC1 = \frac{1}{j\omega C1} \cdot I1 = V2 - V1 \quad \cdots (9)$$

Based upon the equations (8) and (9), in association with the first and second differential pairs 12 and 14 of the active filter circuit 10 shown in Fig. 4, the above described equation (7) is established, and therefore, the following equations (10) and (11) are obtainable;

$$\frac{V3 - V2}{2re1} \cdot \frac{1}{j\omega C1} = V2 - V1 \quad \cdots (10)$$

$$\frac{V5 - V2}{2re2} \cdot \frac{1}{j\omega C2} = V3 - V4 \quad \cdots (11)$$

where re2 is a differential resistor, that is, emitter resistor of each of the transistors Q21 and Q22 of the second differential pair 14.

In accordnce with the above described equations (10) and (11), if the voltage V3 is eliminated while $j\omega = S$, the following equation (12) is obtained.

$$\frac{V5 - V2}{2re2} \cdot \frac{1}{SC2} + V4 - V2 = 2rel\ SC1(V2 - V1)$$

$$V5 - V2 + 2re2\ SC2(V4 - V2) = 4rel\ re2\ S^2\ C1C2(V2 - V1)$$

$$V5 - 2re2\ SC2V4 + 4rel\ re2\ S^2\ C1C2V1$$

$$= V2 + 2re2\ SC2V2 + 4rel\ re2\ S^2\ C1C2V2 \quad \cdots(12)$$

Now, if the terminals 18 and 22 are connected to the ground and a signal is inputted to the terminal 24, V1 = V4 = 0 and V5 = Vin are obtained, and therefore, a transfer function $T_{(s)}$ of the active filter circuit 10 of Fig. 4 is given by the following equation (13).

$$T(s) = \frac{\dfrac{1}{4rel\ re2\ C1C2}}{S^2 + S\dfrac{2re2\ C2}{4rel\ re2\ C1C2} + \dfrac{1}{4rel\ re2\ C1C2}} \quad \cdots(13)$$

The equation (13) shows a secondary lowpass function. A cut-off frequency ω c thereof is given by the following equation (14) and Q is given by the following equation (15).

(15).

$$\omega o = \sqrt{\frac{1}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(14)$$

$$Q = \sqrt{\frac{rel\ C1}{re2\ C2}} = \sqrt{\frac{I2C1}{I1C2}} \quad \cdots(15)$$

Thus, the active filter circuit 10 of Fig. 4 is implemented as a secondary lowpass filter.

Similarlily, when a signal is inputted to the terminal 18 and the terminals 22 and 24 are connected to the ground, V1 = Vin and V4 = V5 = 0 are obtained, and therefore, a transfer function $T_{(s)}$ thereof is given by the following equation (16) which shows a secondary highpass function. Then, a cut-off frequency ω c is given by the following equation (17) and Q is given by the following equation (18).

$$T(s) = \frac{s^2}{s^2 + s\,\dfrac{2re2\ C2}{4rel\ re2\ C1C2} + \dfrac{1}{4rel\ re2\ C1C2}} \quad \cdots(16)$$

$$\omega c = \sqrt{\frac{1}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(17)$$

$$Q = \sqrt{\frac{rel\ C1}{re2\ C2}} = \sqrt{\frac{I2C1}{I1C2}} \quad \cdots(18)$$

Thus, the active filter circuit 10 of Fig. 4 is implemented as a secondary highpass filter.

In addition, if the terminals 18 and 24 are connected to the ground and a signal is inputted to the terminal 22, V1 = V5 = 0 and V4 = Vin are obtained, and therefore, a secondary band-pass filter having a center frequency ω o and Q respectively represented by the following equations (19) and (20) is obtainable.

$$\omega o = \sqrt{\frac{1}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(19)$$

$$Q = \sqrt{\frac{rel\ C1}{re2\ C2}} = \sqrt{\frac{I2C1}{I1C2}} \quad \cdots(20)$$

In addition, if a signal is simultaneously inputted to the terminals 18 and 24 and the terminal 22 is connected to the ground, V1 = V5 = Vin and V4 = 0 are obtained, and therefore, it is possible to obtain a secondary band elimination filter having a center frequency ω o and Q respectively represented by the following equations (21) and (22).

$$\omega o = \sqrt{\frac{1}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(21)$$

$$Q = \sqrt{\frac{rel\ C1}{re2\ C2}} = \sqrt{\frac{I2C1}{I1C2}} \quad \cdots(22)$$

Furthermore, if a signal is simultaneously inputted to the terminals 18 and 24 and a signal reversed in phase is inputted to the terminal 22, V1 = V5 = Vin and V4 = -Vin are obtained, and therefore, it is possible to implement a secondary phase-shifting circuit having a center frequency ω o, Q and a phase characteristic respectively represented by the following equations (23), (24) and (25).

$$\omega o = \sqrt{\frac{1}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(23)$$

$$Q = \sqrt{\frac{rel\ C1}{re2\ C2}} = \sqrt{\frac{I2C1}{I1C2}} \quad \cdots(24)$$

$$\arg T(j\omega) = -2\tan^{-1}\frac{\omega o\omega}{Q(\omega o^2 - \omega^2)} \quad \cdots(25)$$

Thus, in accordance with Fig. 4 embodiment, different kinds of secondary filter circuits can be implemented by the same circuit configuration. Therefore, in a case where a plurality of different kinds of filter circuits are incorporated within the same IC, if the control voltages Vc to be applied to the terminals 26 of the respective filters are linkaged with each other by adjusting only a single control voltage, it is possible to adjust all the filter circuits without any fluctuations.

With reference to Fig. 5, an active filter circuit 10′ of this embodiment utilizes two differential pairs 12 and 14 each having the same configuration as that of the differential pair 1 described in Fig. 2A to 2C. A feed-back voltage V1 from a second differential pair 14 is applied to a (+) input of a first differential pair 12′ (corresponding to the base input of the transistor Q1 in Fig. 2B), and a voltage V2 is applied to a (-) input therefof (corresponding to the base input of the transistor Q2 in Fig. 2B). Voltages V1 and V4 are respectively applied to capacitive loads of the differential pairs 12′ and 14, that is, capacitors C1 and C2. To a (+) input of the second differential pair 14 (corresponding to the base input of the transistor Q1 in Fig. 2B), a voltage V5 is applied, and an output voltage V3 of the first differential pair 12′ is applied to a (-) input thereof (corresponding to the base input of the transistor Q2 in Fig. 2B).

The active filter circuit 10′ of Fig. 5 is specifically shown in Fig. 6. The active filter circuit 10′ of Fig. 6 is different from Fig. 4 embodiment in the following points. More specifically, in Fig. 4 embodiment, the negative feed-back path is formed between the output and the input of the transistor Q12 constituting the first differential pair 12. However, in the active filter circuit 10′ of Fig. 6 embodiment, a base input (- input) of the transistor Q12 constituting the first differential pair 12′ is connected to the terminal 20 and has no negative feed-back path. In addition, the output of the second differential pair 14 is connected to the

terminal 18. However, since the remaining points of Fig. 6 embodiment are the same or similar to that of Fig. 4 embodiment, a duplicate description will be omitted here.

Now, it is assumed that voltages at the terminals 18, 20, 28, 22 and 24 are respectively set as V1, V2, V3, V4 and V5.

As similar to Fig. 4 embodiment, when the voltage V5 at the terminal 24 increases, a collector current of the transistor Q22 decreses, and a current of the transistor Q24 increases by that decreased amount, and therefore, the output voltage V1 of the transistor Q24 increases. When the voltage V1 increases, a collector current of the transistor Q12 decreases, and a current of the transistor Q14 increases by that decreased amount, and therefore, the voltage V2 at the terminal 20 increases. When the voltage V2 increases, the decrease of the collector currents of the transistors Q12 and Q22 are suppressed so that operations of the first and second differential pairs 12′ and 14 become stable. Therefore, each of the first and second differential pairs 12′ and 14 always operates in the vicinity of a center of a renear region thereof, and therefore, no distortion of the signals occurs and a good filter characteristic is obtainable.

In association with the first and second differential pairs 12′ and 14 of the active filter circuit 10′ shown in Fig. 6, by modifying the above described equation (7), the following equations (26) and (27) are obtainable.

$$\frac{V1 - V2}{2rel} \cdot \frac{1}{j\omega C1} = V3 - V1 \quad \cdots(26)$$

$$\frac{V5 - V3}{2re2} \cdot \frac{1}{j\omega C2} = V1 - V4 \quad \cdots(27)$$

In accordnce with the above described equations (26) and (27), if the voltage V3 is eliminated while $j\omega = S$, the following equation (28) is obtained.

$$V5 - \left(\frac{V1 - V2}{2rel} \cdot \frac{1}{SC1} + V1\right) = 2rel\ SC1(V1 - V4)$$

$$V2 - V1 + 2rel\ SC1(V5 - V1) = 4rel\ re2\ S^2\ C1C2(V1 - V4)$$

$$V2 + 2rel\ SC1V5 + 4rel\ re2\ S^2\ C1C2V4$$

$$= V1 + 2rel\ SC1V1 + 4rel\ re2\ S^2\ C1C2V1 \quad \cdots(28)$$

Now, if the terminals 22 and 24 are connected to the ground and a signal is inputted to the terminal 20, V4 = V5 = 0 and V2 = Vin are obtained, and therefore, a transfer function $T_{(s)}$ of the active filter circuit 10′ of Fig. 6 is given by the following equation (29).

$$T_{(s)} = \frac{\dfrac{1}{4rel\ re2\ C1C2}}{S^2 + S\dfrac{2rel\ C1}{4rel\ re2\ C1C2} + \dfrac{1}{4rel\ re2\ C1C2}} \quad \cdots(29)$$

The equation (29) shows a secondary lowpass function. A cut-off frequency ω c thereof is given by the following equation (30) and Q is given by the following equation (31).

$$\omega c = \sqrt{\frac{1}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(30)$$

$$Q = \sqrt{\frac{re2\ C2}{rel\ C1}} = \sqrt{\frac{I1C2}{I2C1}} \quad \cdots(31)$$

Thus, the active filter circuit 10' of Fig. 6 is implemented as a secondary lowpass filter.

Similarlily, when a signal is inputted to the terminal 22 and the terminals 20 and 24 are connected to the ground, V4 = Vin and V2 = V5 = 0 are obtained, and therefore, a transfer function $T_{(s)}$ thereof is given by the following equation (32) which shows a secondary highpass function. Then, a cut-off frequency ω c is given by the following equation (33) and Q is given by the following equation (34).

$$T(s) = \frac{S^2}{S^2 - S\dfrac{2re2\ C2}{4rel\ re2\ C1C2} - \dfrac{1}{4rel\ re2\ C1C2}} \quad \cdots(32)$$

$$\omega c = \sqrt{\frac{1}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(33)$$

$$Q = \sqrt{\frac{re2\ C2}{rel\ C1}} = \sqrt{\frac{I1C2}{I2C1}} \quad \cdots(34)$$

Thus, the active filter circuit 10' of Fig. 6 is implemented as a secondary highpass filter.

In addition, if the terminals 20 and 22 are connected to the ground and a signal is inputted to the terminal 24, V2 = V4 = 0 and V5 = Vin are obtained, and therefore, a secondary band-pass filter having a center frequency ω o and Q respectively represented by the following equations (35) and (36) is obtainable.

$$\omega o = \sqrt{\frac{1}{4re1\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(35)$$

$$Q = \sqrt{\frac{re2\ C2}{re1\ C1}} = \sqrt{\frac{I1C2}{I2C1}} \quad \cdots(36)$$

In addition, if a signal is simultaneously inputted to the terminals 20 and 22 and the terminal 24 is connected to the ground V2 = V4 = Vin and V5 = 0 are obtained, and therefore, it is possible to obtain a secondary band elimination filter having a center frequency ω o and Q respectively represented by the following equations (37) and (38).

$$\omega o = \sqrt{\frac{1}{4re1\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(37)$$

$$Q = \sqrt{\frac{re2\ C2}{re1\ C1}} = \sqrt{\frac{I1C2}{I2C1}} \quad \cdots(38)$$

Furthermore, if a signal is simultaneously inputted to the terminals 20 and 22 and a signal reversed in phase is inputted to the terminal 24, V2 = V4 = Vin and V5 = -Vin are obtained, and therefore, it is possible to implement a secondary phase-shifting circuit having a center frequency ω o, Q and a phase characteristic respectively represented by the following equations (39), (40) and (41).

$$\omega o = \sqrt{\frac{1}{4re1\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \quad \cdots(39)$$

$$Q = \sqrt{\frac{re2\ C2}{re1\ C1}} = \sqrt{\frac{I1C2}{I2C1}} \quad \cdots(40)$$

$$\arg T(j\omega) = -2\tan^{-1}\frac{\omega o\omega}{Q(\omega o^2 - \omega^2)} \quad \cdots(41)$$

Thus, in accordance with Fig. 6 embodiment, different kinds of secondary filter circuits can be

implemented by the same circuit configuration. Therefore, in a case where a plurality of different kinds of filter circuits are incorporated within the same IC, if the control voltages Vc to be applied to the terminals 26 of the respective filters are linkaged with each other by adgusting a single control valtage, it is possible to adjust all the filter circuits without any fluctuations.

An active filter circuit 10 as shown in Fig. 7 is a modification of Fig. 4 embodiment and thus the same or similar to Fig. 4 except for the following point. More specifically, the base of the above described transistor Q12 constituting the first differential pair 12 is connected to the emitter of the transistor Q14 constituting the emitter follower through a resistor R1 and a bias voltage 30 through a resistor R2. An output of the transistor Q12, that is, the transistor Q14 is thus fed-back to the base or input of the transistor Q12 through the resistor R1. In addition, the base of the transistor Q11 constituting the first differential pair 12 is connectd to the output of the transistor Q22 constituting the second differential pair 14, that is, the output of the emitter follower transistor Q24 through a resistor R3 and the above described bias voltage source through a resistor R4.

In association with the first and second differential pairs 12 and 14 of the active filter circuit 10 shown in Fig. 7, by modifying the above described equation (7), the following equations (42) and (43) are obtainable;

$$\frac{KV3 - KV2}{2re1} \cdot \frac{1}{j\omega C1} = V2 - V1 \quad \cdots(42)$$

$$\frac{V5 - V2}{2re2} \cdot \frac{1}{j\omega C2} = V3 - V4 \quad \cdots(43)$$

where K is a constant (described later).

In accordnce with the above described equations (42) and (43), if the voltage V3 is eliminated while $j\omega = S$, the following equation (44) is obtained.

$$K\left(\frac{V5 - V2}{2re2} \cdot \frac{1}{SC2} + V4 - V2\right) = 2re1\ SC1(V2 - V1)$$

$$V5 - V2 - 2re2\ SC2(V4 - V2) = \frac{1}{K} 4re1\ re2\ S^2\ C1C2(V2 - V1)$$

$$V5 - 2re2\ SC2V4 = V2 - 2re2\ SC2V2 - \frac{1}{K} 4re1\ re2\ S^2\ C1C2V2$$

$$K = \frac{R4}{R3 + R4} = \frac{R2}{R1 + R2} \quad \cdots(44)$$

Now, if the terminals 18 and 22 are connected to the ground and a signal is inputted to the terminal 24, V1 = V4 = 0 and V5 = Vin are obtained, and therefore, a transfer function $T_{(s)}$ of the active filter circuit 10 of Fig. 7 is given by the following equation (45).

$$T(s) = \frac{\dfrac{K}{4rel\ re2\ C1C2}}{s^2 + s\dfrac{2re2\ C2\ K}{4rel\ re2\ C1C2} + \dfrac{K}{4rel\ re2\ C1C2}} \quad \cdots(45)$$

The equation (45) shows a secondary lowpass function. A cut-off frequency ωc thereof is given by the following equation (46) and Q is given by the following equation (47).

$$\omega c = \sqrt{\frac{K}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}\cdot K} \quad \cdots(46)$$

$$Q = \frac{1}{\sqrt{K}}\sqrt{\frac{rel\ C1}{re2\ C2}} = \frac{1}{\sqrt{K}}\sqrt{\frac{I2C1}{I1C2}} \quad \cdots(47)$$

Thus, the active filter circuit 10 of Fig. 7 is implemented as a secondary lowpass filter.

Similarlily, when a signal is inputted to the terminal 18 and the terminals 22 and 24 are connected to the ground, V1 = Vin and V4 = V5 = 0 are obtained, and therefore, a transfer function $T_{(s)}$ thereof is given by the following equation (48) which shows a secondary highpass function. Then, a cut-off frequency ωc is given by the following equation (49) and Q is given by the following equation (50).

$$T(s) = \frac{\dfrac{K}{4rel\ re2\ C1C2}}{s^2 + s\dfrac{2re2\ C2\ K}{4rel\ re2\ C1C2} + \dfrac{K}{4rel\ re2\ C1C2}} \quad \cdots(48)$$

$$\omega c = \sqrt{\frac{K}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}\cdot K} \quad \cdots(49)$$

$$Q = \frac{1}{\sqrt{K}}\sqrt{\frac{rel\ C1}{re2\ C2}} = \frac{1}{\sqrt{K}}\sqrt{\frac{I2C1}{I1C2}} \quad \cdots(50)$$

Thus, the active filter circuit 10 of Fig. 7 is implemented as a secondary highpass filter.

In addition, if the terminals 18 and 24 are connected to the ground and a signal is inputted to the terminal 22, V1 = V5 = 0 and V4 = Vin are obtained, and therefore, a secondary band-pass filter having a center frequency ωo and Q respectively represented by the following equations (51) and (52) is obtainable.

$$\omega o = \sqrt{\frac{K}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \cdot K \quad \cdots(51)$$

$$Q = \frac{1}{\sqrt{K}}\sqrt{\frac{rel\ C1}{re2\ C2}} = \frac{1}{\sqrt{K}}\sqrt{\frac{I2C1}{I1C2}} \quad \cdots(52)$$

In addition, if a signal is simultaneously inputted to the terminals 18 and 24 and the terminal 22 is connected to the ground V1 = V5 = Vin and V4 = 0 are obtained, and therefore, it is possible to obtain a secondary band elimination filter having a center frequency ω o and Q respectively represented by the following equations (53) and (54).

$$\omega o = \sqrt{\frac{K}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \cdot K \quad \cdots(53)$$

$$Q = \frac{1}{\sqrt{K}}\sqrt{\frac{rel\ C1}{re2\ C2}} = \frac{1}{\sqrt{K}}\sqrt{\frac{I2C1}{I1C2}} \quad \cdots(54)$$

Furthermore, if a signal is simultaneously inputted to the terminals 18 and 24 and a signal reversed in phase is inputted to the terminal 22, V1 = V5 = Vin and V4 = -Vin are obtained, and therefore, it is possible to implement a secondary phase-shifting circuit having a center frequency ω o, Q and a phase characteristic respectively represented by the following equations (55), (56) and (57).

$$\omega o = \sqrt{\frac{K}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}} \cdot K \quad \cdots(55)$$

$$Q = \frac{1}{\sqrt{K}}\sqrt{\frac{rel\ C1}{re2\ C2}} = \frac{1}{\sqrt{K}}\sqrt{\frac{I2C1}{I1C2}} \quad \cdots(56)$$

$$\arg T(j\omega) = -2\tan^{-1}\frac{\omega o\omega}{Q(\omega o^2 - \omega^2)} \quad \cdots(57)$$

Thus, In accordance with Fig. 7 embodiment, if the constant K determined by the resistors R1 to R4 of

the base biases of the transistors Q11 and Q12, the above described respective filter characteristics can be modified, and it is further possible to adjust a filter characteristic by means of a control voltage Vc applied to the terminal 26.

Fig. 8 embodiment is a modification of Fig. 7 embodiment, and an active filter circuit 10 of Fig. 8 embodiment is different from Fig. 7 embodiment in the following points. More specifically, in Fig. 7 embodiment, the base of the transistor Q12 constituting the first differential pair 12 is connected to the emitter of the transistor Q14 through the resistor R1 and the bias voltage source 30 through the resistor R2, and the base of the transistor Q11 constituting the first differential pair 12 is connected to the emitter of the transistor Q24 through the resistor R3 and the bias voltage source 30 through the resistor R4. However, in the active filter circuit 10 of Fig. 8 embodiment, the bases of the transistors Q11 and Q12 constituting the first differential pair 12 are respectively connected to the emitters of the transistors Q14 and Q24 through resistors R11 and R13 and interconnected to each other through a resistor R12, which has no bias voltage source.

In Fig. 7 embodiment, the current I1 flowing the transistors Q11 and Q12 are exactly represented by the following equation (58).

$$I1 = \frac{\dfrac{R4}{R3 + R4} V3 + \dfrac{R2}{R1 + R2} V2}{2re1} \quad \cdots (58)$$

Assuming that R2/(R1 + R2) = K1 and R4/(R3 + R4) = K2, even if these resistors are arranged to be close to each other, a ratio of the resistors in the same IC has an error of approximately 2 %, and therefore, a relative ratio of K1 and K2 bocomes to have an error of approximately 4 %.

On the other hand, in Fig. 8 embodiment, assuming that the base voltages of respective transistors Q11 and Q12 are V11 and V12, V11 and V12 are respectively given by the following equations (59) and (60).

$$V11 = \frac{R11 + R12}{R11 + R12 + R13} V3 + \frac{R13}{R11 + R12 + R13} V2 \quad \cdots (59)$$

$$V12 = \frac{R12 + R13}{R11 + R12 + R13} V2 + \frac{R11}{R11 + R12 + R13} V3 \quad \cdots (60)$$

In Fig. 8, a current I1' flowing the transistors Q11 and Q12 is given by the following equation (61) as similar to the current I1 in Fig. 7.

$$I1' = \frac{V11 - V12}{2re1}$$

$$= \frac{(R11 + R12)V3 + R13V2 - (R13 + R12)V2 - R11V3}{(R11 + R12 + R13)\cdot 2re1}$$

$$= \frac{\frac{R12}{R11 + R12 - R13}V3 - \frac{R12}{R11 + R12 + R13}}{2re1} \quad \cdots(61)$$

As seen from the equation (61) coefficients of the voltages V3 and V2 are equal to each other, and therefore, no influence due to an error of the resistance ratio is affected and no bias voltage source is needed. In addition, when R11 = R1, R13 = R3 and R12 = R2 + R4, each of K1 and K2 becomes to be equal to K in Fig. 7.

In addition, Fig. 9 embodiment is a modification of Fig. 7 embodiment, which is differs from Fig. 7 embodiment in that resistors R5 to R8 are connected in association with the transistors Q21 and Q22 of the second differential pair 14. In addition, a transistor Q28 constitutes an emitter follower.

In an active filter circuit 10 as shown in Fig. 9, assuming that an emitter resistor of each of the transistors Q11 and Q12 is re1, a current flowing respective one of the transistors Q11 and Q12 constituting the first differential pair is given by the following equation (62);

$$I1 = \frac{K2\ V3 - K1\ V2}{2re1} \quad \cdots(62)$$

where K1 and K2 are constants (described later).

A signal voltage VC1 of the capacitor C1 is given by the following equation (63).

$$VC1 = \frac{1}{j\omega C1}\cdot I1 = V2 - V1 \quad \cdots(63)$$

The following equation (64) is obtainable by the above described equations (62) and (63). Similarlily, in association with the second differential pair 14, the following equation (65) is obtainable.

$$\frac{K2V3 - K1V2}{2re1}\cdot\frac{1}{j\omega C1} = V2 - V1 \quad \cdots(64)$$

$$\frac{K4V5 - K3V2}{2re2}\cdot\frac{1}{j\omega C2} = V3 - V4 \quad \cdots(65)$$

In accordnce with the above described equations (64) and (65), if the voltage V3 is eliminated while $j\omega = S$, the following equation (66) is obtained.

$$K2\left(\frac{K4V5 - K3V2}{2re2} \cdot \frac{1}{SC2} + V4\right) - K1V2 = 2rel\ SC1(V2 - V1)$$

$$K2K4V5 + K2 \cdot 2re2\ SC2V4 + 4rel\ re2\ S^2\ C1C2V1$$

$$= K2K3V2 + K1 \cdot 2re2\ SC2V2 + 4rel\ re2\ S^2\ C1C2V2$$

$$K1 = \frac{R2}{R1 + R2}$$

$$K2 = \frac{R4}{R3 + R4}$$

$$K3 = \frac{R6}{R5 + R6}$$

$$K4 = \frac{R8}{R7 + R8} \quad \cdots(66)$$

Now, if a signal is simultaneously inputted to the terminals 18 and 20 and the terminal 22 is connected to the ground, V1 = V5 = Vin and V4 = 0 are obtained, and therefore, a transfer function $T_{(s)}$ of the active filter circuit 10 of Fig. 9 is given by the following equation (67).

$$T(s) = \frac{S^2 + \dfrac{K2K4}{4rel\ re2\ C1C2}}{S^2 + S\dfrac{K1 \cdot 2re2\ C2}{4rel\ re2\ C1C2} + \dfrac{K2K3}{4rel\ re2\ C1C2}} \quad \cdots(67)$$

The equation (67) shows a secondary lowpass and band elimination function. A cut-off frequency ω c thereof is given by the following equation (68), Q is given by the following equation (69) and a center frquency ω_N of the band elimination is given by the following equation (70).

$$\omega c = \sqrt{\frac{K2K3}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}\cdot K2K3} \quad \cdots(68)$$

$$Q = \sqrt{\frac{K2K3}{K1^2}\cdot\frac{rel\ C1}{re2\ C2}} = \sqrt{\frac{K2K3}{K1^2}\cdot\frac{I2C1}{I1C2}} \quad \cdots(69)$$

$$\omega N = \sqrt{\frac{K2K4}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}\cdot K2K4} \quad \cdots(70)$$

In a case of $\omega_N > \omega c$, the active filter circuit shown in Fig. 9 becomes as a lowpass and band elimination filter (lowpass notch filter) and in a case of $\omega N < \omega c$, the same becomes as a highpass and band elimination filter (hightpass notch filter).

In a case where K1 = K2 and K3 = K4, as similar to the previously described embodiments, it is possible to implement a lowpass filter, band-pass filter, band elimination filter or phase-shifting filter circuit.

In Fig. 9 embodiment, as seen from the above equations (68) and (70), a lowpass notch filter or a highpass notch filter can be implemented by making values of K3 and K4 different from each other. However, in Fig. 7 embodiment, as seen from the circuit diagram thereof and the aforementioned equation (44), since the signal inputted to the second differential pair 14 is not divided, it is impossible to implement such a lowpass notch filter or highpass notch filter.

Fig. 10 embodiment is an example in which the same change as the first differential pair 12 in Fig. 8 embodiment is applied to the second differential pair 14 by means of resistors R14 to R16, and it is possible to obtain an advantage that no influence due to an error of the resistance ratio is affected, as similar to the aforementioned Fig. 8 embodiment.

Fig. 11 embodiment is a modification of Fig. 6 embodiment, wherein the same change as the first differential pair 12 in Fig. 7 embodiment is applied to the second differential pair 14.

In Fig. 11 embodiment, the aforementioned equation (28) is modified as the following equation (71).

$$V2 + 2rel\ SC1V4 + 4rel\ re2\ S^2\ C1C2\cdot -V5\ \frac{1}{K}$$

$$= V1 + 2rel\ SC1V1 + 4rel\ re2\ S^2\ C1C2\cdot -V1\ \frac{1}{K}$$

$$K = \frac{R6}{R5 + R6} = \frac{R8}{R7 + R8} \quad \cdots(71)$$

Now, if the terminals 22 and 24 are connected to the ground and a signal is inputted to the terminal 20, V1 = V4 = 0 and V5 = Vin are obtained, and therefore, a transfer function $T_{(s)}$ of the active filter circuit 10' of Fig. 11 is given by the following equation (72).

$$T(s) = \frac{\dfrac{K}{4rel\ re2\ C1C2}}{S^2 + S\dfrac{2rel\ C1\ K}{4rel\ re2\ C1C2} + \dfrac{K}{4rel\ re2\ C1C2}} \quad \cdots(72)$$

The equation (72) shows a secondary lowpass function. A cut-off frequency ωc thereof is given by the following equation (73) and Q is given by the following equation (74).

$$\omega c = \sqrt{\frac{K}{4rel\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}\cdot K} \quad \cdots(73)$$

$$Q = \frac{1}{\sqrt{K}}\sqrt{\frac{re2\ C2}{rel\ C1}} = \frac{1}{\sqrt{K}}\sqrt{\frac{I1C2}{I2C1}} \quad \cdots(74)$$

Thus, the active filter circuit 10' of Fig. 11 is implemented as a secondary lowpass filter.

In addition, it is possible to implement a highpass filter, band-pass filter, band elimination filter or phase-shifting filter by Fig. 11 circuit, however, respective characteristics thereof can be easily understood from the above description, and therefore, more detail descriptions will be omitted here.

Fig. 12 is an embodiment in which the same change as the first differential pair 12 of Fig. 8 is applied to the second differential pair 14.

Fig. 13 embodiment is an embodiment wherein the same change of the second differential pair 14 in Fig. 11 embodiment is applied to the first differential pair 12' of Fig. 11 embodiment, too.

More specifically, Fig. 13 embodiment is a modification of Fig. 11 embodiment, as similar to the equations (26) and (27), the following equations (75) and (76) are obtainable.

$$\frac{K4V5 - K3V3}{2re2}\cdot\frac{1}{j\omega C2} = V1 - V4 \quad \cdots(76)$$

$$\frac{K2V1 - K1V2}{2rel}\cdot\frac{1}{j\omega C1} = V3 - V1 \quad \cdots(75)$$

In accordnce with the above described equations (75) and (76), if the voltage V3 is eliminated while $j\omega = S$, the following equation (77) is obtained.

$$K1K3V2 + K4 \cdot 2rel\ SC1V5 + 4rel\ re2\ S^2\ C1C2V4$$

$$= K2K3V1 + K3 \cdot 2rel\ SC2V1 + 4rel\ re2\ S^2\ C1C2V1$$

$$K1 = \frac{R2}{R1 - R2}$$

$$K2 = \frac{R4}{R3 + R4}$$

$$K3 = \frac{R6}{R5 + R6}$$

$$K4 = \frac{R8}{R7 + R8} \qquad \cdots(77)$$

Now, if a signal is simultaneously inputted to the terminals 20 and 22 and the terminal 24 is connected to the ground, V2 = V4 = Vin and V5 = 0 are obtained, and therefore, a transfer function $T_{(s)}$ of the active filter circuit 10 of Fig. 13 is given by the following equation (78).

$$T_{(s)} = \frac{S^2 + \dfrac{K1K3}{4rel\ re2\ C1C2}}{S^2 + S\dfrac{K3 \cdot 2rel\ C1}{4rel\ re2\ C1C2} + \dfrac{K2K3}{4rel\ re2\ C1C2}} \qquad \cdots(78)$$

The equation (78) shows a secondary lowpass and band elimination function. A cut-off frequency ω c thereof is given by the following equation (79), Q is given by the following equation (80) and a center frequency of the band elimination is given by the following equation (81).

$$\omega_C = \sqrt{\frac{K2K3}{4re1\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}\cdot K2K3} \quad \cdots(79)$$

$$Q = \sqrt{\frac{K2K3}{K3^2}\cdot\frac{re1\ C1}{re2\ C2}} = \sqrt{\frac{K2}{K3}\cdot\frac{I1C1}{I2C2}} \quad \cdots(80)$$

$$\omega_N = \sqrt{\frac{K1K3}{4re1\ re2\ C1C2}} = \frac{q}{2kT}\sqrt{\frac{I1I2}{C1C2}\cdot K1K3} \quad \cdots(81)$$

In a case of $\omega_N > \omega_C$, the active filter circuit 10' shown in Fig. 13 becomes as a lowpass and band elimination filter (lowpass notch filter) and in a case of $\omega_N < \omega_C$, the same becomes as a highpass and band elimination filter (hightpass notch filter).

In a case where K1 = K2 and K3 = K4, as similar to Fig. 6 embodiment, it is possible to implement a lowpass filter, band-pass filter, band elimination filter or phase-shifting filter circuit.

In Fig. 13 embodiment, as seen from the above equations (79) and (81), a lowpass notch filter or a highpass notch filter can be implemented by making values of K1 and K2 different from each other. However, in Fig. 11 embodiment, as seen from the circuit diagram thereof and the aforementioned equation (39), since the signal inputted to the second differential pair 14 is not divided, it is impossible to implement such a lowpass notch filter or highpass notch filter.

In addition, in respective embodiments shown in Fig. 14, the input (base) voltages of the transistors constituting the first differential pair 12' is applied by the voltage-dividing by means of three resistors R14 to R16, as similar to Fig. 10 embodidment, and therefore, it is possible to eliminate an influence due to a fluctuation of bias resistors of the respective transistors in Fig. 13 embodiments. However, a duplicate description will be omitted here.

All the above described embodiments are secondary active filter circuits 10 or 10'; however, the present invention is also applicable to a tertiary or more active filter circuit 100 as shown in Fig. 15A to Fig. 15D.

Active filter circuits 100 shown by Fig. 15A to Fig. 15D are specifically constructed as shown in Fig. 16A to Fig. 16D, respectively.

In an active filter circuit 100 as shown in Fig. 16A, a current flowing respective one of the transistors Q11 and Q12 constituting the first differential pair 12 is given by the following equation (82).

$$I1 = \frac{V1 - V2}{2re1} \quad \cdots(82)$$

A signal voltage VC11 of the capacitor C11 is given by the following equation (83).

$$VC11 = \frac{1}{j\omega C1}\cdot I1 = V3 - V4 \quad \cdots(83)$$

The following equation (84) is obtainable by the above described equations (82) and (83).

$$\frac{V1 - V2}{2re1} \cdot \frac{1}{j\omega C11} = V3 - V4 \quad \cdots(84)$$

Similarlily, in association with the second and third differential pairs, the following equations (85) and (86) are obtained.

$$\frac{V3 - V2}{2re2} \cdot \frac{1}{j\omega C12} = V5 - V6 \quad \cdots(85)$$

$$\frac{V5 - V2}{2re3} \cdot \frac{1}{j\omega C13} = V2 - V7 \quad \cdots(86)$$

In accordnce with the above described equations (84), (85) and (86), if the voltages V3 and V4 are eliminated while $j\omega = S$, the following equation (87) is obtained.

$$\frac{V1 - V2}{2re1} \cdot \frac{1}{SC11} + V4 - V2 = 2re2\ SC12(V2 - V6)$$

$$+ 4re2\ re3\ S^2\ C12C13(V2 - V7)$$

$$V1 - V2 + 2re1\ SC11(V4 - V2) = 4re1\ re2\ S^2C11C12(V2 - V6)$$

$$+ 8re1\ re2\ re3\ S^3\ C11C12C13V7$$

$$V1 - 2re1SC11V2 + 4re1\ re2\ S^2\ C11C12V6$$

$$- 8re1\ re2\ re3S^3\ C11C12C13V7 = V2 - 2re1SC11V2$$

$$- 4re1\ re2\ S^2C11C12V2 - 8re1\ re2\ re3\ S^3C11C12C13V7 \quad \cdots(87)$$

Now, if a signal is simultaneously inputted to the terminals 22 and 34 and a signal reversed in phase is simultaniously inputted to the terminals 18 and 32, V4 = V7 = Vin and V1 = V6 = -Vin are obtained, and therefore, a transfer function $T_{(s)}$ of the active filter circuit 100 of Fig. 16A is given by the following equation (88) which shows a tertiary phase-shifting circuit.

$$T_{(s)} = \frac{S^3 + S^2 + \frac{4re1re2C11C12}{A} + S\frac{2re1C11}{A} - \frac{1}{A}}{S^3 + S^2 + \frac{4re1re2C11C12}{A} + S\frac{2re1C11}{A} - \frac{1}{A}}$$

$$A = 8re1\ re2\ re3\ C11C12C13 \quad \cdots(88)$$

In addition, in Fig. 16B to Fig. 16D, similarlily, it is possible to obtain tertiary filter circuits; however, the details thereof can be easily understood by those skilled in the art, and therefore, detail descriptions thereof are omitted here. In addition, it is needless to say that in the active filter circuit 100 shown in Fig. 16A to Fig. 16D, as similar to the previous active filter circuits 10 or 10′, resistor circuits for voltage-dividing the input voltage may be added thereto.

The above described active filter circuits 10, 10′ or 100 shown by Fig. 4, Fig. 6 to Fig. 14, and Fig. 16A to Fig. 16D can be utilized as follows.

Fig. 17 is a block diagram showin a PLL (phase Locked Loop) as another embodiment in accordance with the present invention, in which the active filter circuit 10, 10′ or 100 is utilized as a bandpass filter 40.

In Fig. 17, an output of the bandpass filter 40 is fed-back through an amplifier 42 so that the output is in phase with an input thereof and a gain thereof becomes 1 or more, whereby an oscillator is constructed. A center frequency of the bandpass filter 40 is controlled to construct a VCO (Voltage Controlled Oscillator) 44.

If a phase between the input and output of the amplifier 42 is the same and a gain of a closed loop of the VCO 44 is 1 or more, since a phase difference between the input and the output at the center frequency of the bandpass filter 40 is 0° (in the same phase), the VCO 44 oscillates at the center frequency of the bandpass filter 40. A signal obtained by the VCO 44 is phase-compared with an input signal in a phase comparator 46.

When only a direct current voltage component is derived from a signal outputted from the phase-comparator 46 by a lowpass filter 48, a control voltage Vc in accordance with a phase difference between an oscillation signal of the VCO 44 and the input signal is obtained. If the control voltage Vc is fed-back to the terminal 26 shown in Fig. 4 and the like, the VCO 44 is controlled so that the output thereof becomes to have the same frequency as that of the input signal.

Thus, the VCO can be incorporated within the IC, and in a case where a plurality of different kinds of filter circuits are further incorporated within the same IC, if the control voltages Vc to be applied to the terminals 26 (Fig. 4) of the respective filters or circuits are linkaged with each other by adjusting a single control voltage, it is possible to adjust all the filter circuits without no scattering.

Fig. 18 and Fig. 19 are block diagrams respectively showin embodiments to each of which a crystal filter 50 is added. The crystal filter 50 is a filter for setting a center frequency of the VCO 44.

Fig. 20 is a block diagram showing a chroma circuit as another embodiment in accordance with the present invention. In the NTSC standard, a video signal is inputted to a input terminal 52, which is inputted in turn to a chroma demodulation circuit 58 and a phase comparator 46 through a 3.58 MHz bandpass filter 54 and an amplifier 56. A signal outputted from a 3.58 MHz VCO 60 is inputted to the phase comparator 46 to be phase-comparated with the video signal previously inputted (burst). When only a direct current component is derived from a signal outputted from the phase-comparator 46 by the lowpass filter 48, a voltage in accordance with a phase difference between the input video signal (burst) and the output signal of the 3.58 MHz VCO 60 is outputted as a control voltage Vc. If the control voltage Vc is fed-back to the terminal 26 as shown in Fig. 4 and etc., a center frequency of the bandpass filter 54 becomes equal to that of the input video signal (burst), and therefore, a frequency of the output signal of the 3.58 MHz VCO 60 also becomes equal to that of the input video signal (burst). The output signal of the 3.58 MHz VCO 60 is inputted to the chroma demodulation circuit 58, and thus, the input video signal is demodulated and outputted as a color difference signal.

In addition, the video signal inputted to the input terminal 52 is inputted in turn to a video processing circuit 64 through a 3.58 MHz trap circuit 62, and the input video signal is outputted as a luminance signal after various kinds of video processings.

In Fig. 20 embodiment, the 3.58 MHz bandpass filter 54, a 3.58 MHz bandpass filter (not shown) within the 3.58 MHz VCO 60 and the 3.58 MHz trap circuit 62 are implemented with the same active filter circuit 10, 10′ or 100 as shown in Fig. 4, and etc., and therefore, when the aforementioned control voltage Vc is applied to the control voltages of these filters or circuits, the characteristics thereof can be automatically adjusted to desired characteristics.

Fig. 21 is a block diagram showing a circuit for automatically controlling a phase-shifting filter in a quadrature detection as another embodiment in accordance with the present invention. An FM signal input is applied to a phase-shifting filter 68 and a multiplier 70 from an input terminal 66. An output of the phase-shifting filter 68 is also applied to the multiplier 70. Then, an output of the multiplier 70 is withdrawn at an output terminal 74 through a lowpass filter 72 as a demodulated output. More specifically, in the quadrature detection, as well known, the FM signal input is multiplied with a signal being phase-shifted by the phase-shifting filter 68 in the multiplier 70 and, when a phase difference between both the signals is 90°, a reference voltage Vref is obtained and the demodulate output which is changed in a form of a so-called S-

curve in which the reference voltage is a center thereof.

It is to be noted that the output of the multiplier 70 is applied to a lowpass filter 76 and an output of the lowpass filter 76 is applied to a level comparator 78. The lowpass filter 76 is a filter for deriving only a direct current voltage in accordane with a phase difference of the output from the multiplier 70 and the output thereof is applied to the level comparator 78 together with the reference voltage Vref. Then, a control voltage Vc in accordance with a level-difference between the output V of the lowpass filter 76 and the reference voltage Vref is applied to the above described phase-shifting filter 68 from the level comparator 78.

In addition, as the phase-shifting filter 68 in Fig. 21 embodiment, the active filter circuit 10, 10′ or 100 as shown in Fig. 4 and etc. may be utilized.

In Fig. 21, in a case where a characteristic of the phase-shifting filter 68 is deviated from a desired characteristic and the phase difference does not become 90° at a predetermined frequency fo, only a direct current voltage component is derived from the signal outputted from the multiplier 70 by the lowpass filter 76, the voltage V in accordance with the such a deviation of the filter characteristic from reference voltage Vref is outputted as the control voltage Vc. If the control voltage Vc is fed-back to the terminal 26 as shown in Fig. 4 and etc., the phase-shifting filter 68 is automatically controlled so that an output phase difference becomes 90°.

In addition, a method for FM detection is not limited by the above described quadrature detection system, may be other arbitrary system.

Fig. 22 is a block diagram showing a VIF and SIF circuit as another embodiment in accordance with the present invention.

In a television receiver of the NTSC standard, a VIF signal is inputted to the input terminals 80 and 82, which is applied in turn to a video detection circuit 86 through a VIF amplifier 84. In the video detection circuit 86, the VIF signal is detected to output a video signal component which becomes a video output through a 4.5 MHz trap circuit 88.

In addition, an output of the video detection circuit 86 is applied to a 4.5 MHz bandpass filter 90 an output of which is applied to a 4.5 MHz discriminator 94 through a limitter amplifier 92. Then, an output of the 4.5 MHz discriminator 94 is applied to an FM detection circuit 96. On the other hand, an output of the limitter 92 is applied to the FM detection circuit 96 as it is. Then, an audio output as demodulated is obtained from the FM detection circuit 96.

It is noted that an output of the FM detection circuit 96 is applied to a level comparator 98 to which a reference voltage Vref is further applied.

In addition, in Fig. 22 embodiment, as the 4.5 MHz trap circuit 88, 4.5 MHz bandpass filter 90 and 4.5 MHz discriminator 94, as described in the above, the same active filter circuit 10, 10′ or 100 as shown in Fig. 4, and etc. may be utilized.

Then, since an SIF signal is an FM wave, in Fig. 22, only a direct current voltage component is derived from an output signal which is detected by the FM detection circuit 96 and a voltage V is compared with the reference voltage Vref which is to be a center voltage of an originary S-curve in the level comparator 98. Therefore, in the level comparator 98, as similar to Fig. 21 embodiment, a voltage in accordance with a diviation of the characteristic of the 4.5 MHz discriminator 94 is obtained, which is applied in turn to a control input of the 4.5 MHz discriminator 94 as a control voltage Vc. Then, in this embodiment shown, since the 4.5 MHz trap circuit 88 and 4.5 MHz bandpass filter 90 are implemented with filter circuits having the same circuit configuration, the same output of the level comparator 98, that is, the control voltage Vc are applied to these circuits 88 and 90 as the control inputs therefor.

Thus, if the voltage V in accordance with the deviation of the filter characteristic of the 4.5 MHz discriminator 94 and the reference voltage Vref are compared with each other and a difference voltage is applied to the 4.5 MHz discriminator as well as the 4.5 MHz trap circuit 88 and the 4.5 MHz bandpass filter 90 as the control voltage Vc thereof, the characteristics of these filters can be adjusted or controlled uniformly.

In addition, in any of the embodiment shown in Fig. 21 and Fig. 22, the diviation of the output voltage of the S-curve of the FM detection circuit is compared with the reference voltage Vref. However, an active filter can be automatically adjusted or controlled to a desired characteristic even in the IC of the other signal without necessity of the FM detection. In such a case, a phase-shifting filter is to be provided as a dummy filter; however, it is not necessary to use a reference signal as that of the conventional circuit.

Fig. 23 is a block diagram showing the other embodiment in accordance with the present invention. This embodiment shown can be utilized, for example, as an FM circuit for sound recording of a VTR. An output of a crystal bandpass filter 100 is inputted to a bandpass filter 102 an output of which is fed-back to the crystal bandpass filter 100 through an amplifier 104. Therefore, by these components 100, 102 and 104,

a VCO as shown in Fig. 18 or 19 is constructed. An output of the VCO is applied to a phase-shifting filter 106 and a phase comparator 108. The phase-shifting filter 106 is a filter in which an amplitude is a constant irrespective to a frequency and a phase difference between the input and the output can be adjusted to zero at a resonant frequency capable of being controlled from the external. To the phase comparator 108, an output of the phase-shifting filter 106 is further applied. A signal in accordance with a phase difference between both the input signals is outputted from the phase comparator 108 and applied in turn to a lowpass filter 110. The lowpass filter 110 outputs a control voltage Vc in accordance with the above descrined phase difference, which is applied to the phase-shifting filter 106. In addition, the output of the lowpass filter 110 is also added to the control voltage from the external by an adder 112, and a voltage as added is applied to the bandpass filter 102 as a control voltage therefor.

In Fig. 23 embodiment, as the bandpass filter 102 and the phase-shifting filter 106, the active filter circuit 10, 10′ or 100 as shown in Fig. 4 and etc. is utilized.

Then, when the output of the lowpass filter 110, that is, the control voltage Vc is applied to the terminal 26 (Fig. 4 and etc.) of the phase-shifting filter 106, a center frequency of the phase-sifting filter 106 is controlled delicately, resulting in zero of the phase difference between the input and output of the phase-shifting filter 106. Therefore, a resonant frequency of the phase-shifting filter 106 is always coincident with a frequency of an oscillation output from the amplifier 104.

In addition, since the bandpass filter 102 is constructed by the same active filter circuit as that of the phase-shifting filter 106, by feeding-back the output voltage of the lowpass filter 100 to the bandpass filter 102 through the adder 112, a resonant frequency of the bandpass filter 102 is also coincident with an oscillation frequency of the VCO. Then, at that frequency, the phase difference between the input and output of the bandpass filter 102 becomes zero, and therefore, the oscillation frequency of the VCO becomes a resonant frequency of a crystal (not shown) of the crystal bandpass filter 100, and therefore, no harmonic component is included in the oscillation frequency.

Then, by adding an external signal having a frequency sufficiently higher than a cut-off frequency of the lowpass filter 110 to the output voltage of the lowpass filter 110 and applying the same to the bandpass filter 102, a center frequency of the bandpass filter 102 is changed in accordance with the external signal, and therefore, the oscillation output of the VCO can be frequency-modulated by the external control signal.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. An active filter circuit, comprising:
a first differential pair constructed to include a first and second transistors;
a first capacitive load connected to an output of said second transistor of said first differential pair;
a first negative feed-back path for feeding-back an output of said second transistor to an input thereof;
a second differential pair constructed to include a third and fourth transistors;
a second capacitive load connected to an output of said fourth transistor of said second differential pair; and
a second negative feed-back path for feeding-back an output of said fourth transistor to an input of said first transistor constituting said first differential pair.

2. An active filter circuit, comprising:
a first differential pair constructed to include a first and second transistors;
a first capacitive load connected to an output of said second transistor of said first differential pair;
a second differential pair constructed to include a third and fourth transistors;
a connecting path for connecting an output of said second transistor of said first differential pair to an input of said fourth transistor of said second differential pair;
a second capacitive load connected to an output of said fourth transistor; and
a negative feed-back path for feeding-back an output of said fourth transistor to an input of said first transistor constituting said first differential pair.

3. An active filter circuit in accordance with claim 1 or 2, further comprising current changing means for correlatively changing current amounts of said first and second differential pairs in response to a given control voltage.

4. An active filter circuit in accordance with claim 3, further comprising biasing means formed in association with at least one of said first and second differential pairs for applying bias voltages to bases of two transistors constituting said at least one of the differential pairs.

5. An active filter circuit in accordance with claim 4, wherein said biasing means include resistor voltage-dividing means for applying a divided voltage to respective bases of said two transistors as said bias voltages.

6. An active filter circuit in accordance with claim 5, wherein said resistor voltage-dividing means includes a first resistor series connection a series connecting point of which is connected the base of one of said two transistors and a second resistor series connection a series connecting point of which is connected to the base of the other.

7. An active filter circuit in accordance with claim 6, wherein said biasing means includes a bias voltage source, and respective one ends of the two resistor series connections are connected to said bias voltage source.

8. An active filter circuit in accordance with claim 6, wherein said first and second resistor series connections include a common resistor which is interconnected between the bases of said two transistors.

9. A filter controlling circuit, comprising:

filter, a phase characteristic of said filter being able to be changed in accordance with a control voltage;

means for outputting a direct current voltage component in accordance with said phase characteristic of the output of said filter;

level comparing means for comparing said direct current voltage component with a reference voltage; and

means for applying said control voltage to said filter based upon an output of said level comparing means.

10. A filter controlling circuit in accordance with claim 9, wherein said filter includes:

a first differential pair constructed to include a first and second transistors;

a first capacitive load connected to an output of said second transistor of said first differential pair;

a first negative feed-back path for feeding-back an output of said second transistor to an input thereof;

a second differential pair constructed to include a third and fourth transistors;

a second capacitive load connected to an output of said fourth transistor of said second differential pair;

a second negative feed-back path for feeding-back an output of said fourth transistor to an input of said first transistor constituting the first differential pair; and

current changing means for correlatively changing current amounts of said first and second differential pairs in response to said control voltage.

11. A filter controlling circuit in accordance with claim 9, wherein said filter include:

a first differential pair constructed to include a first and second transistors;

a first capacitive load connected to an output of said second transistor of said first differential pair;

a second differential pair constructed to include a third and fourth transistors;

a connecting path for connecting an output of said second transistor of said first differential pair to an input of said fourth transistor of said second differential pair;

a second capacitive load connected to an output of said fourth transistor;

a negative feed-back path for feeding-back an output of said fourth transistor to an input of said first transistor constituting said first differential pair; and

current changing means for correlatively changing current amounts of said first and second differential pairs in response to said control voltage.

12. A filter controlling circuit, comprising:

a filter, a center frequency of said filter being able to be changed in accordance with a control voltage;

amplifying means having a gain of 1 or more for feeding-back an output of said filter to an input of said filter;

phase comparing means receiving the output of said filter and a further input signal; and

means for applying said control voltage to said filter based upon an output of said phase comparing means.

13. A filter controlling circuit in accordance with claim 12, wherein said filter includes:

a first differential pair constructed to include a first and second transistors;

a first capacitive load connected to an output of said second transistor of said first differential pair;

a first negative feed-back path for feeding-back an output of said second transistor to an input thereof;

a second differential pair constructed to include a third and fourth transistors;

a second capacitive load connected to an output of said fourth transistor of said second differential pair;

a second negative feed-back path for feeding-back an output of said fourth transistor to an input of said first transistor constituting said first differential pair; and

current changing means for correlatively changing current amounts of said first and second differential pairs in response to said control voltage.

14. A filter controlling circuit in accordance with claim 12, wherein said filter include:

a first differential pair constructed to include a first and second transistors;

a first capacitive load connected to an output of said second transistor of said first differential pair;

a second differential pair constructed to include a third and fourth transistors;
a connecting path for connecting an output of said second transistor of said first differential pair to an input of said fourth transistor of said second differential pair;
a second capacitive load connected to an output of said fourth transistor;
a negative feed-back path for feeding-back an output of said fourth transistor to an input of said first transistor constituting said first differential pair; and
current changing means for correlatively changing current amounts of said first and second differential pairs in response to said control voltage.

FIG. 1

PRIOR ART

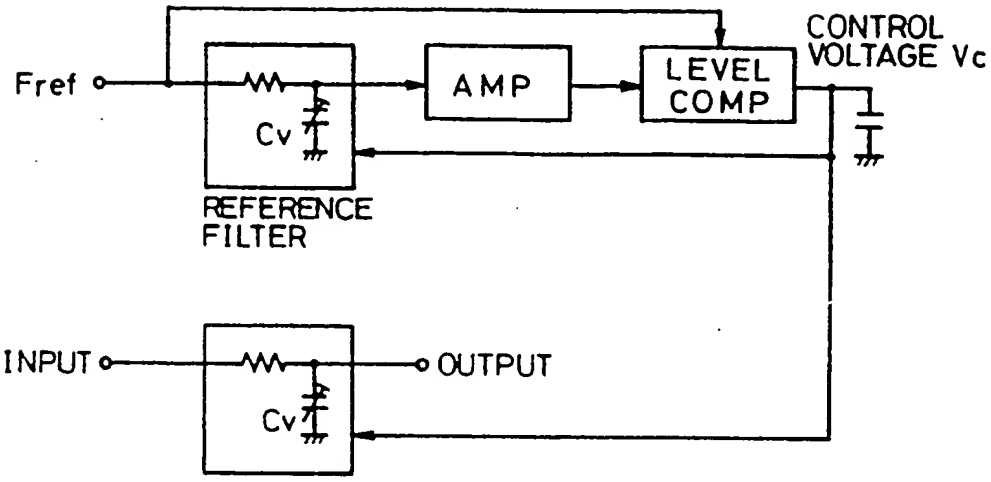


FIG. 2A

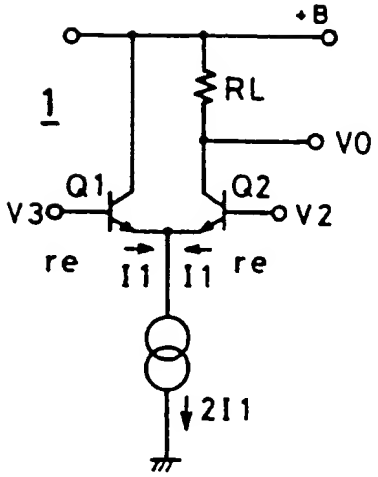


FIG. 2B

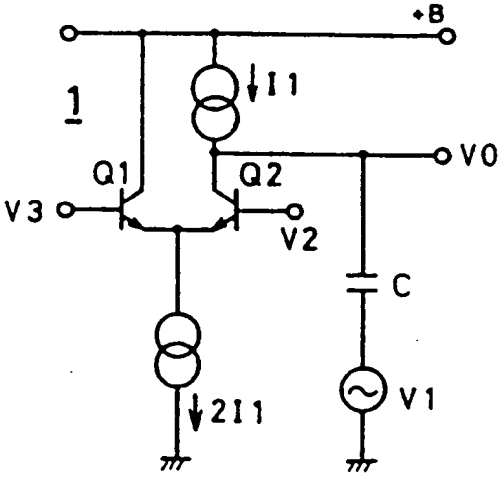


FIG. 2C

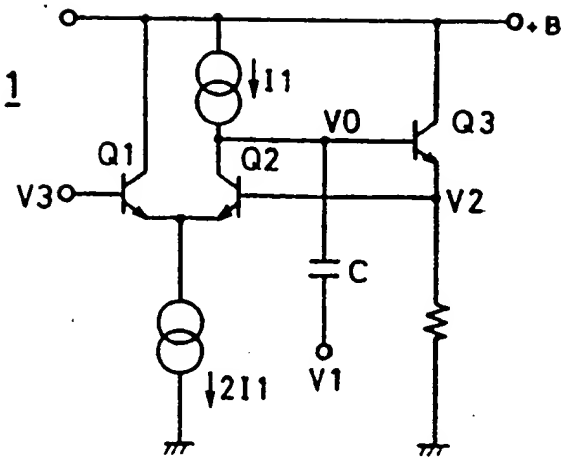


FIG. 3

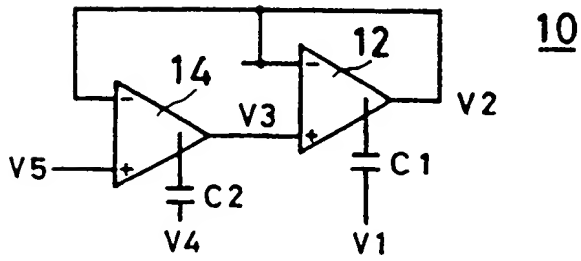


FIG. 4

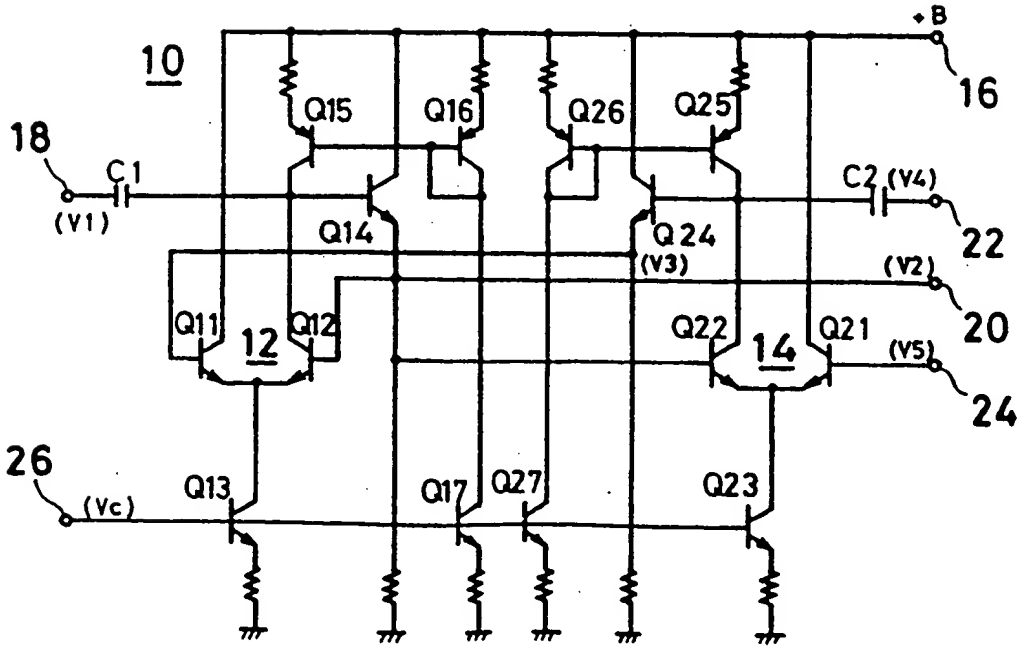
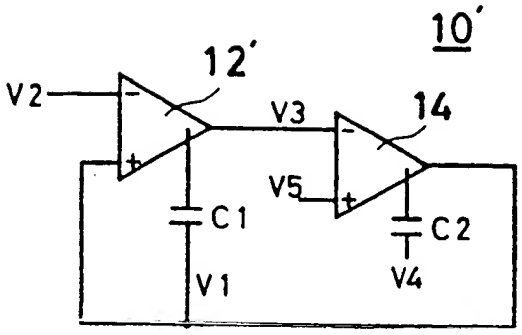


FIG. 5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V3
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V5
C1
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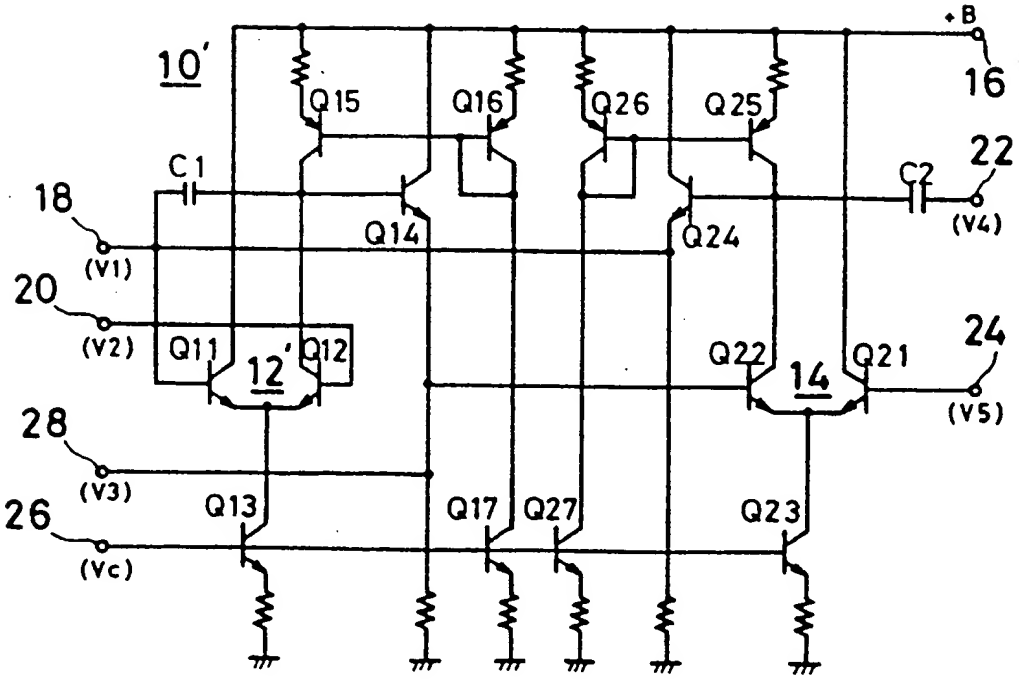
V4

FIG. 6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Q11
12'
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(V3)
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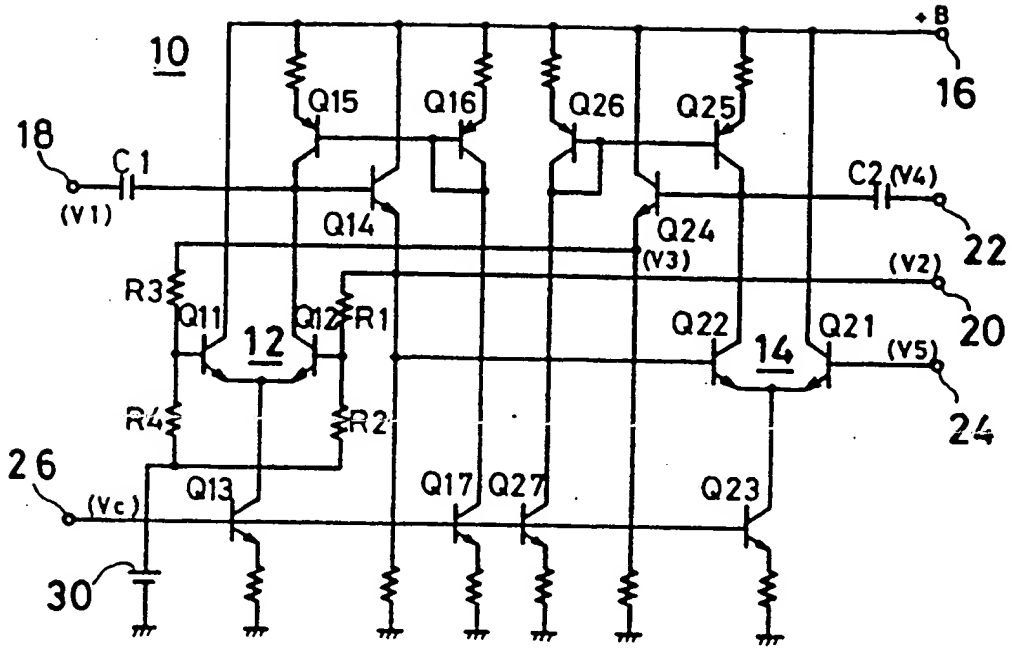
(Vc)
Q13
Q17
Q27
Q23

FIG. 7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20
R3
Q11
12
Q12
R1
Q22
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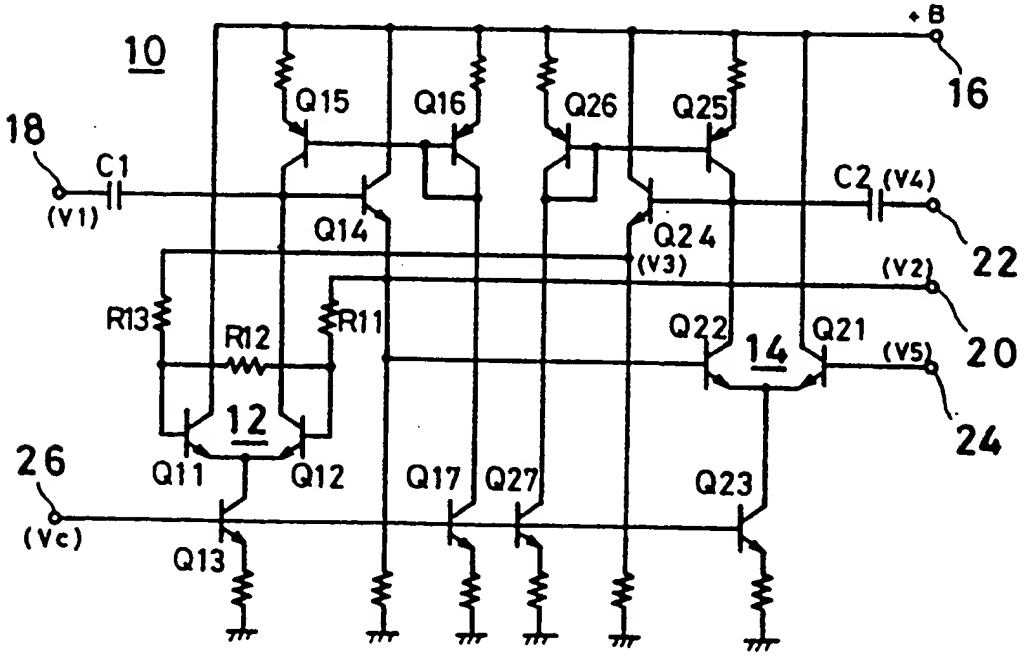
R4
R2
26
(Vc)
Q13
Q17
Q27
Q23
30

FIG. 8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R11
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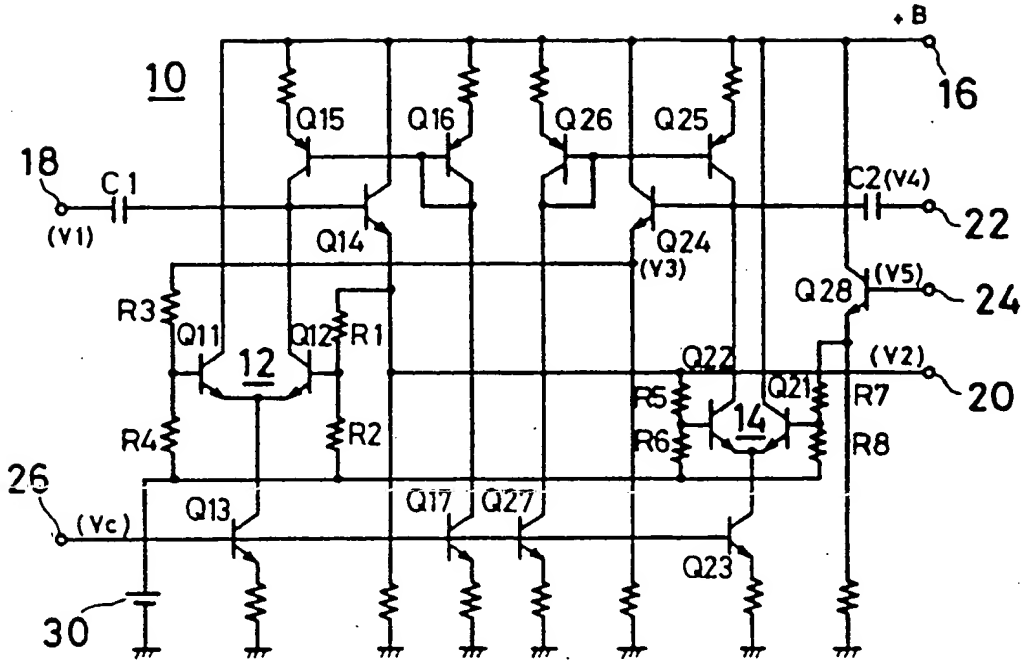
(Vc)
Q13

FIG. 9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R3
Q11
12
Q12
R1
Q22
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20
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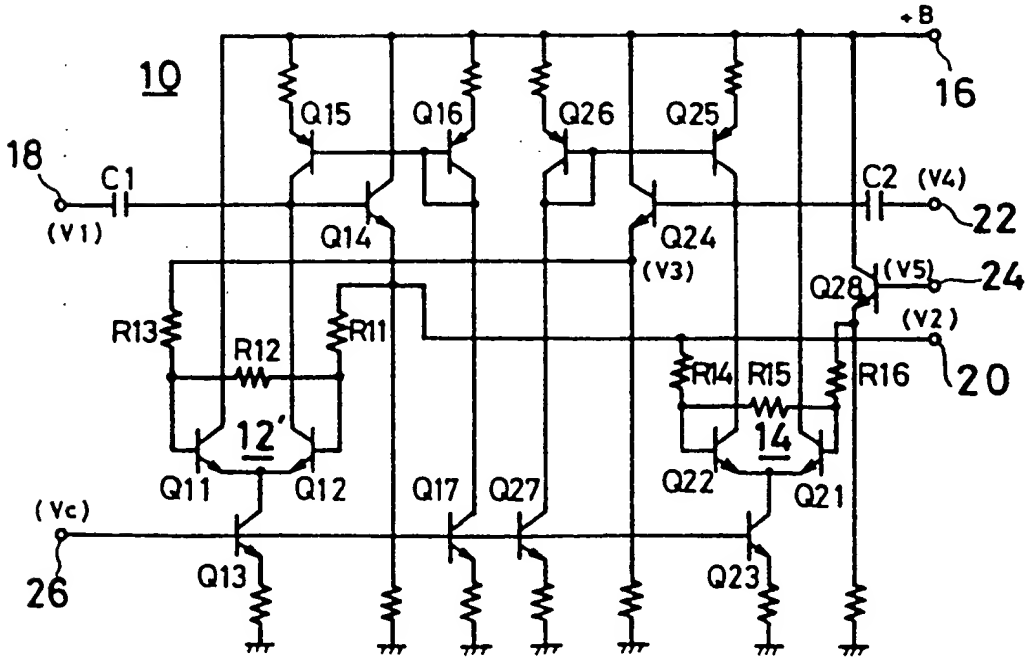
FIG. 10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Q28
(V2)
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R12
R11
R14
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Q23

FIG.11

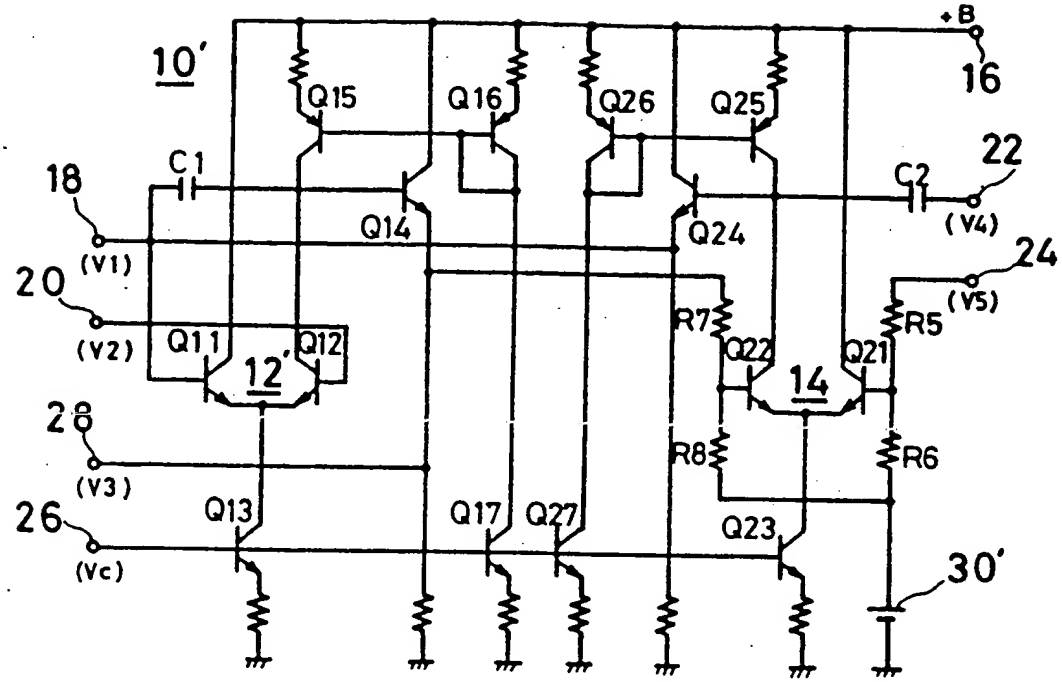
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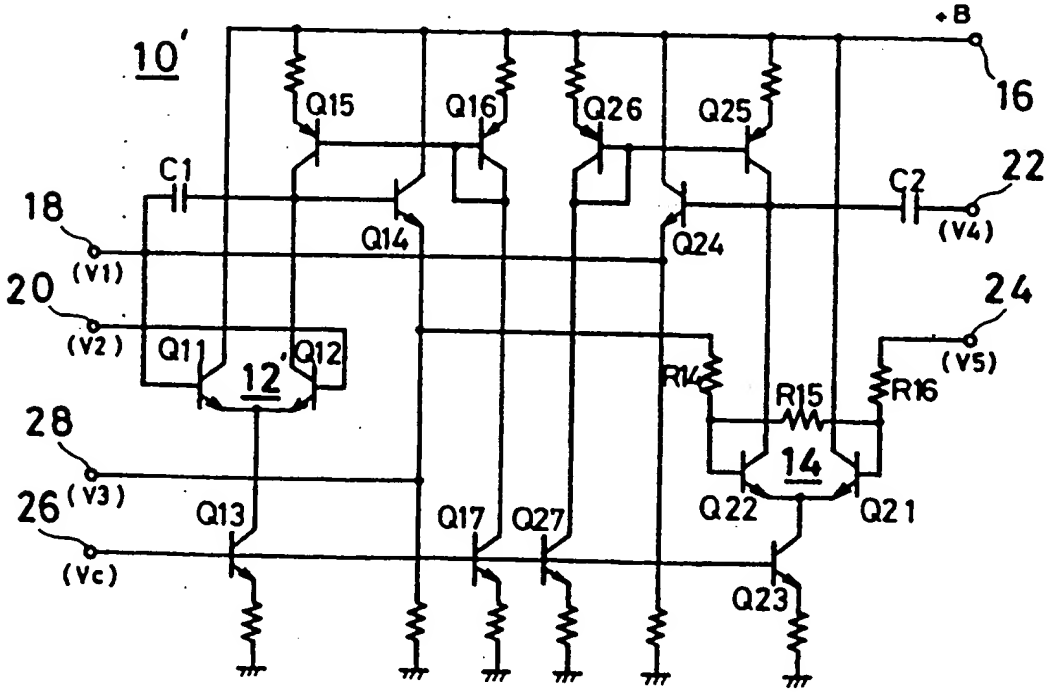
FIG.12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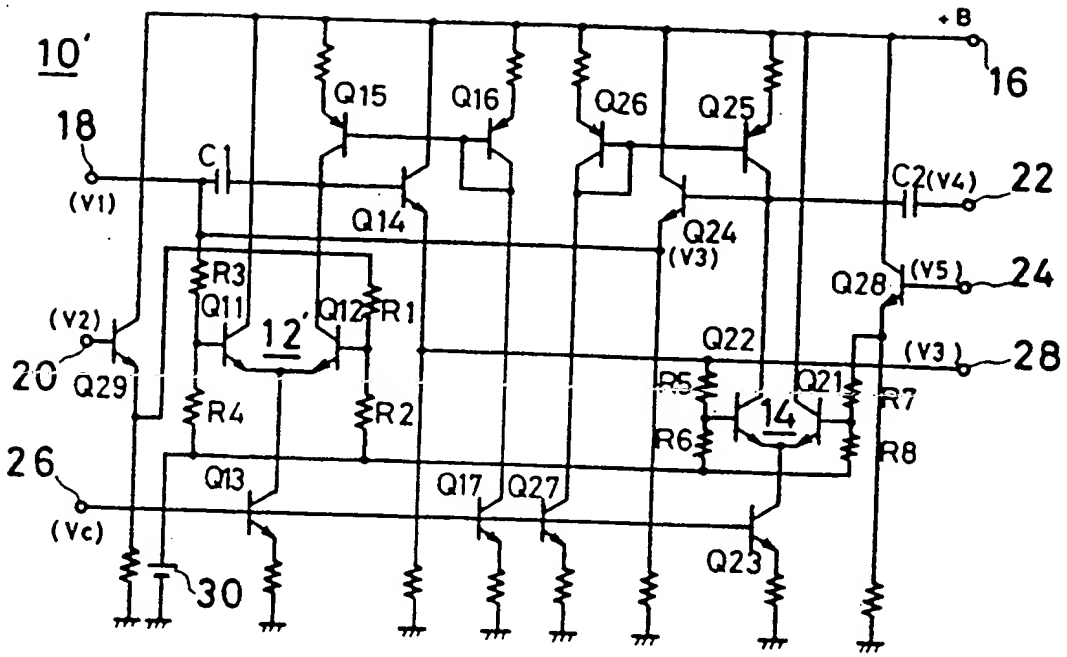
Q22
Q21
(Vc)
Q23

FIG.13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Q25
Q14
Q24
(V3)
R3
Q11
12'
Q12
R1
R4
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Q13
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R6
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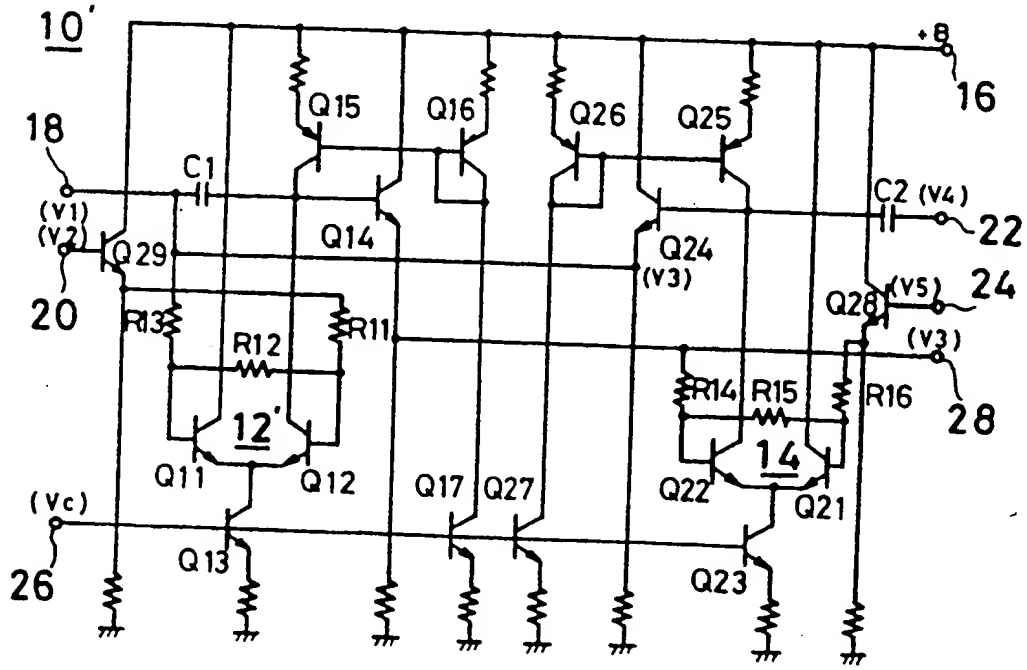
R7
R8

FIG.14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Q21

FIG.15A

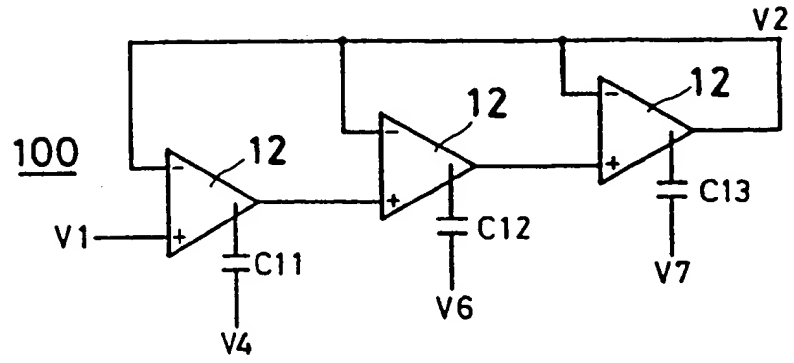


FIG.15B

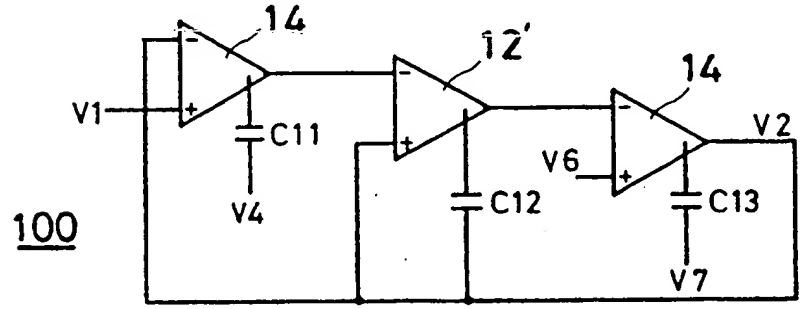


FIG.15C

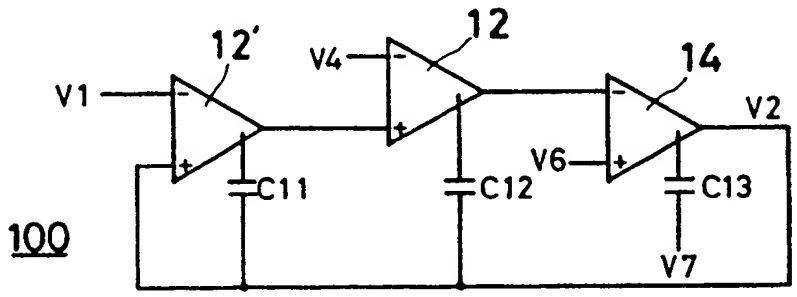


FIG.15D

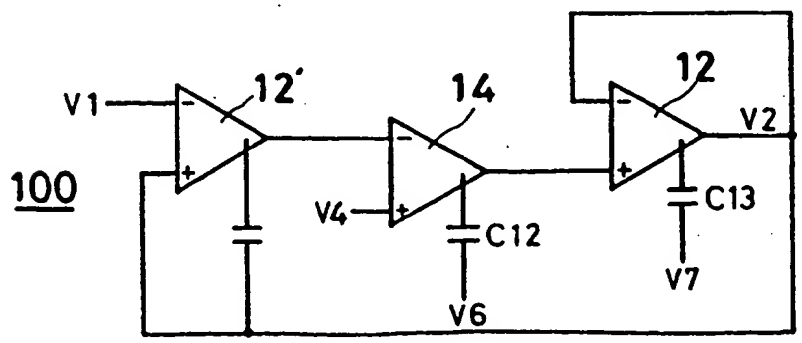


FIG.16A

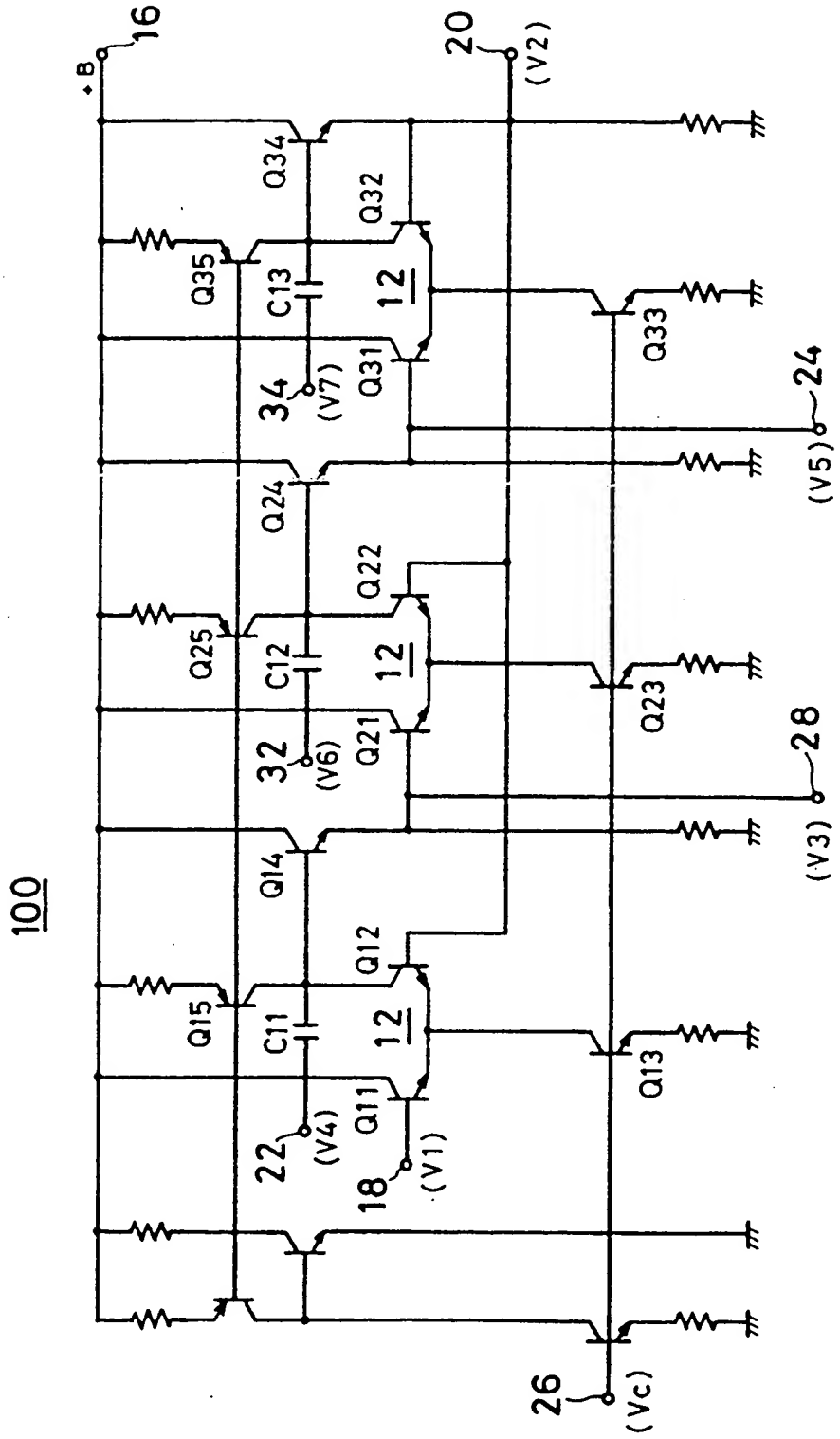

100
+B
16
20
(V2)
Q34
Q32
Q35
C13
12
Q33
34
(V7)
Q31
24
(V5)
Q24
Q22
Q25
C12
12
Q23
32
(V6)
Q21
28
(V3)
Q14
Q12
Q15
C11
12
Q13
22
(V4)
Q11
18
(V1)
26
(Vc)

FIG.16B

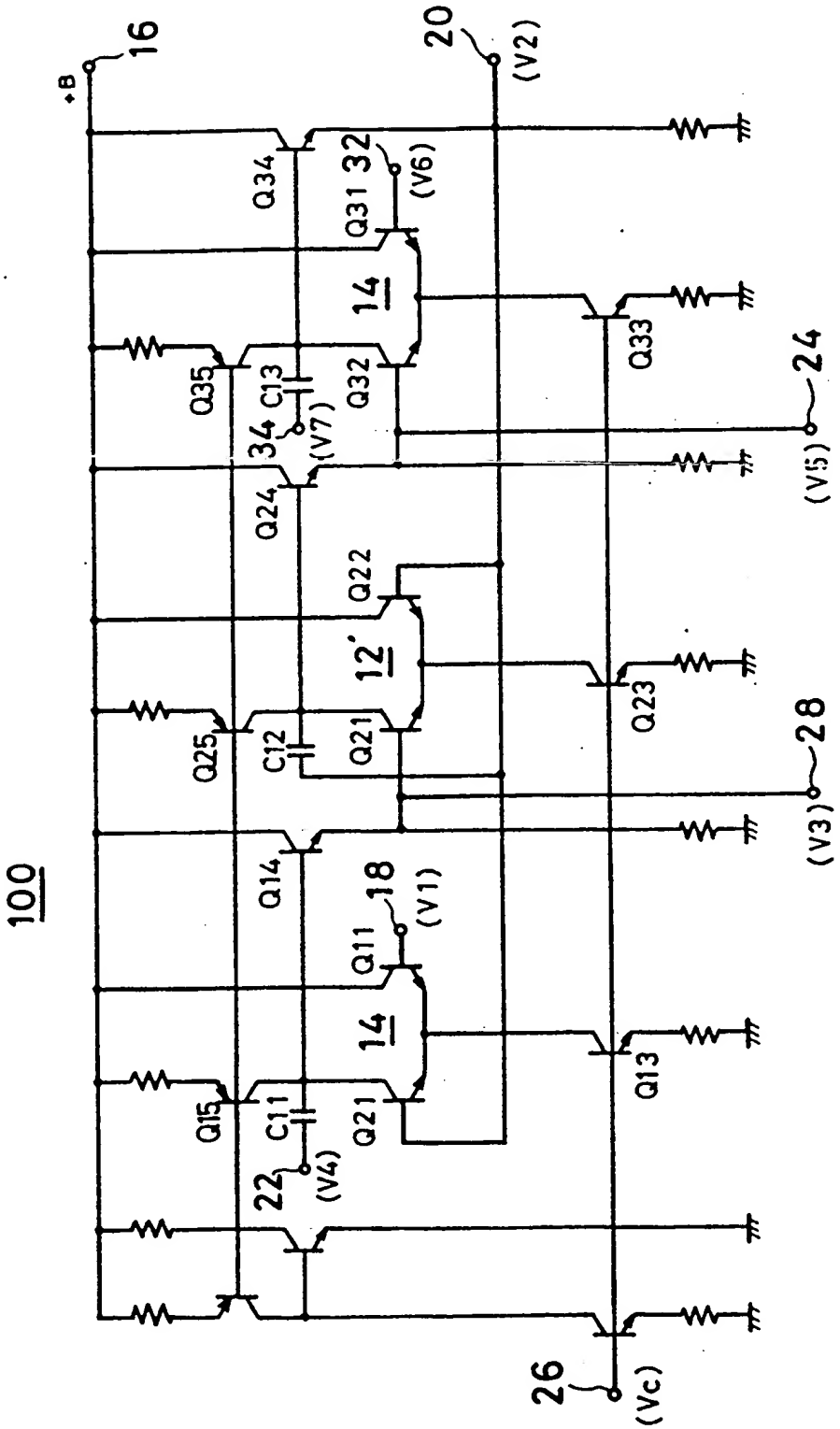
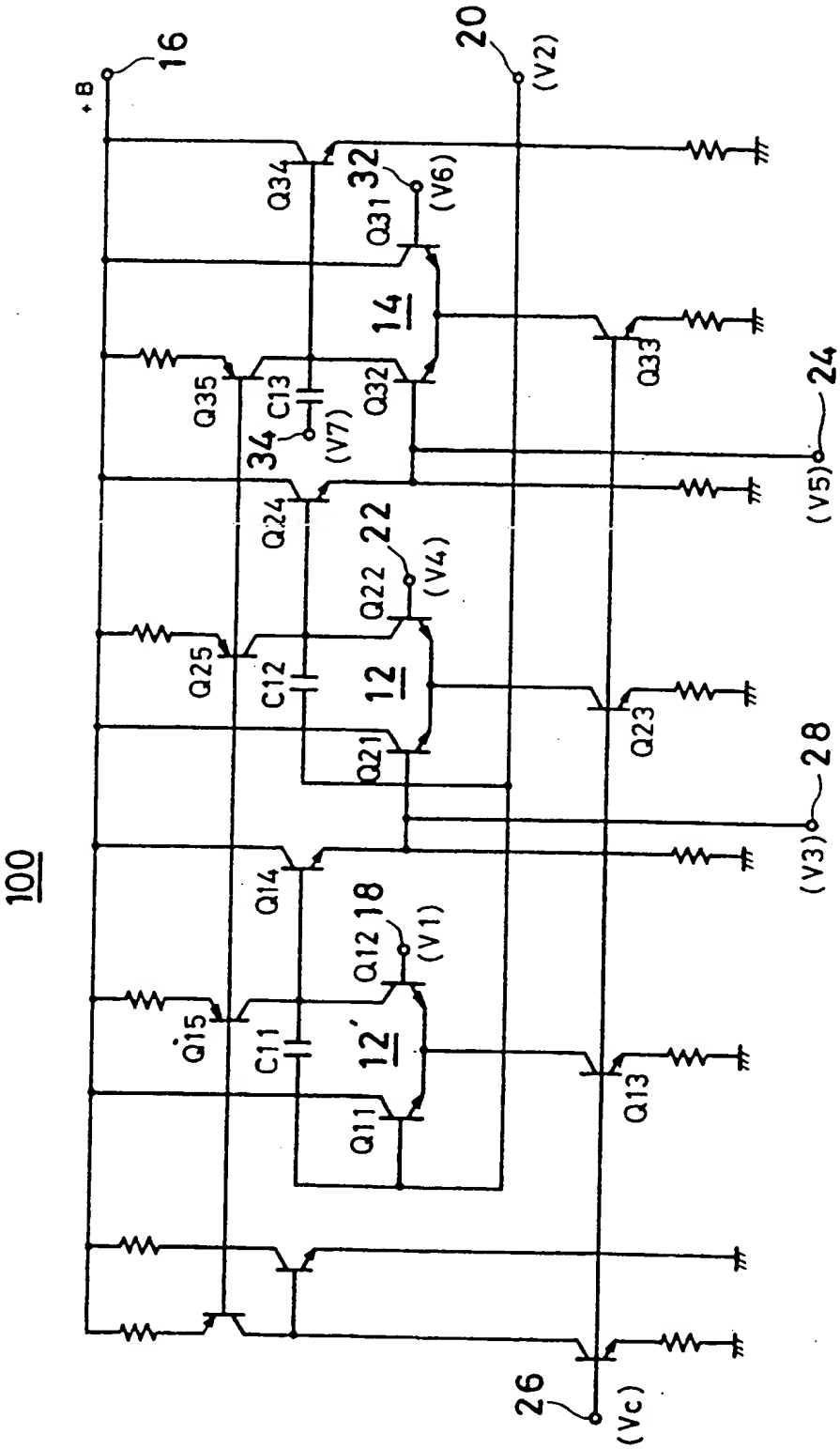

100
+B
16
20
(V2)
Q34
Q31
32
(V6)
14
Q35
C13
Q32
Q33
34
(V7)
24
(V5)
Q24
Q22
12'
Q25
C12
Q21
Q23
28
(V3)
Q14
Q11
18
(V1)
14
Q15
C11
Q21
Q13
22
(V4)
26
(Vc)

FIG.16C


100
+B
16
20
(V2)
Q34
32
Q31
(V6)
14
Q35
C13
Q32
Q33
34
(V7)
24
(V5)
Q24
22
Q22
(V4)
Q25
C12
12
Q23
Q21
28
(V3)
Q14
18
Q12
(V1)
Q15
C11
12'
Q13
Q11
26
(Vc)

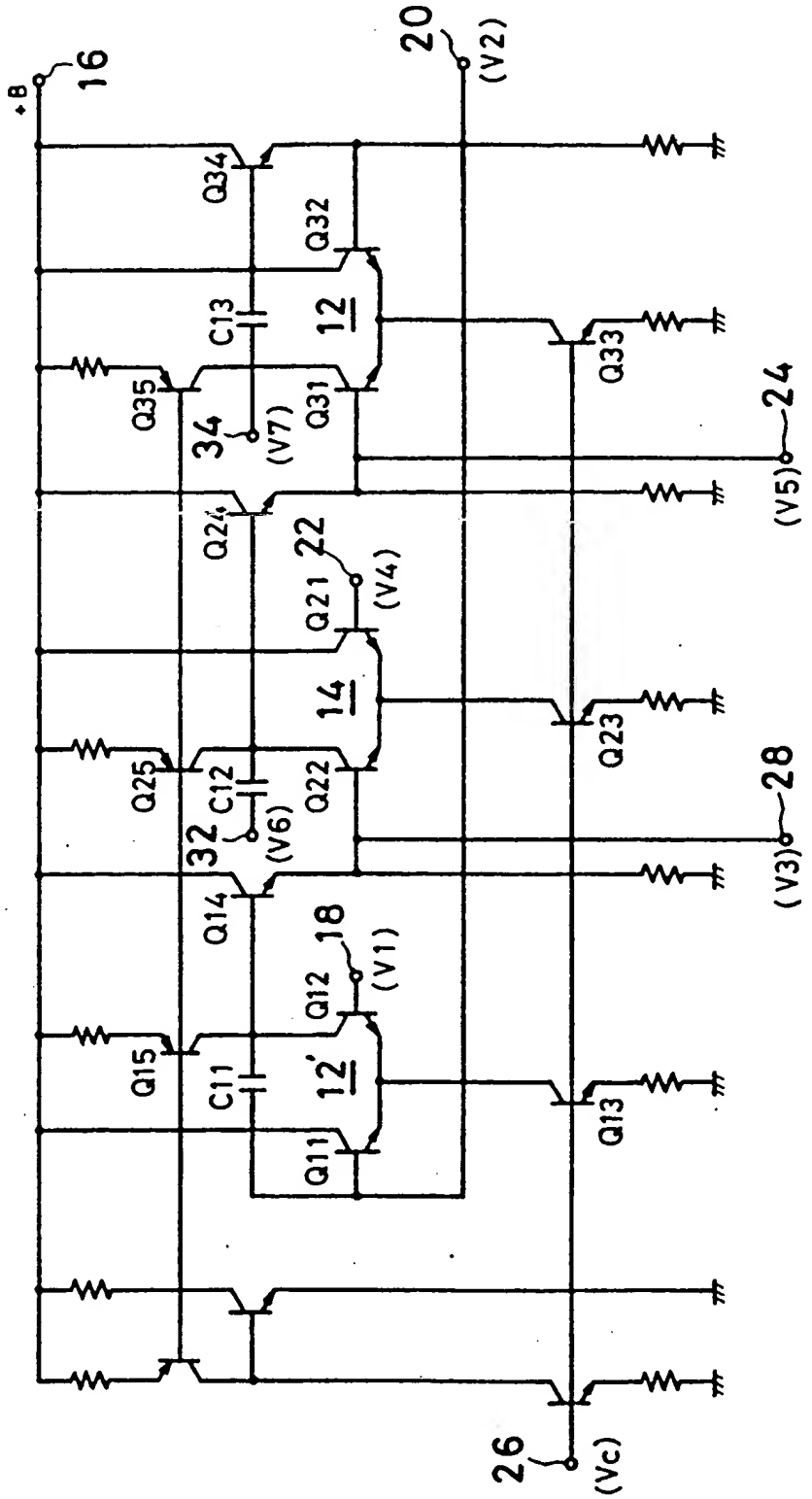

+B
16
20
(V2)
Q34
Q32
C13
12
Q33
Q35
34
(V7)
Q31
24
(V5)
Q24
22
Q21
(V4)
14
Q23
Q25
C12
Q22
32
(V6)
28
(V3)
100
Q14
18
(V1)
Q12
Q15
C11
12'
Q13
Q11
26
(Vc)

FIG.16D

FIG.17

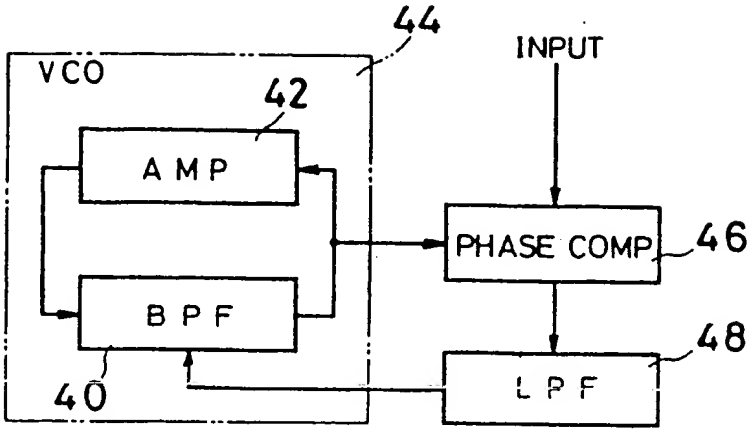

44
INPUT
VCO
42
AMP
PHASE COMP
46
BPF
48
LPF
40

FIG.18

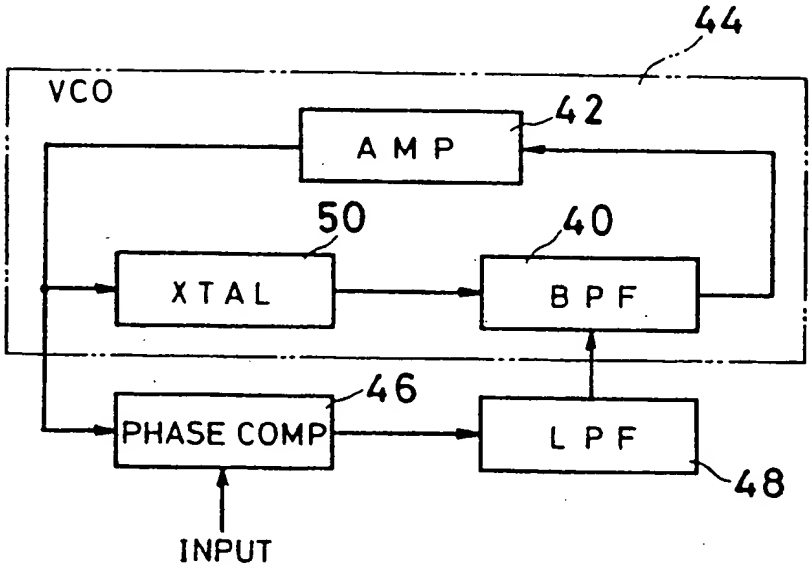

44
VCO
42
AMP
50
40
XTAL
BPF
46
PHASE COMP
LPF
48
INPUT

FIG.19

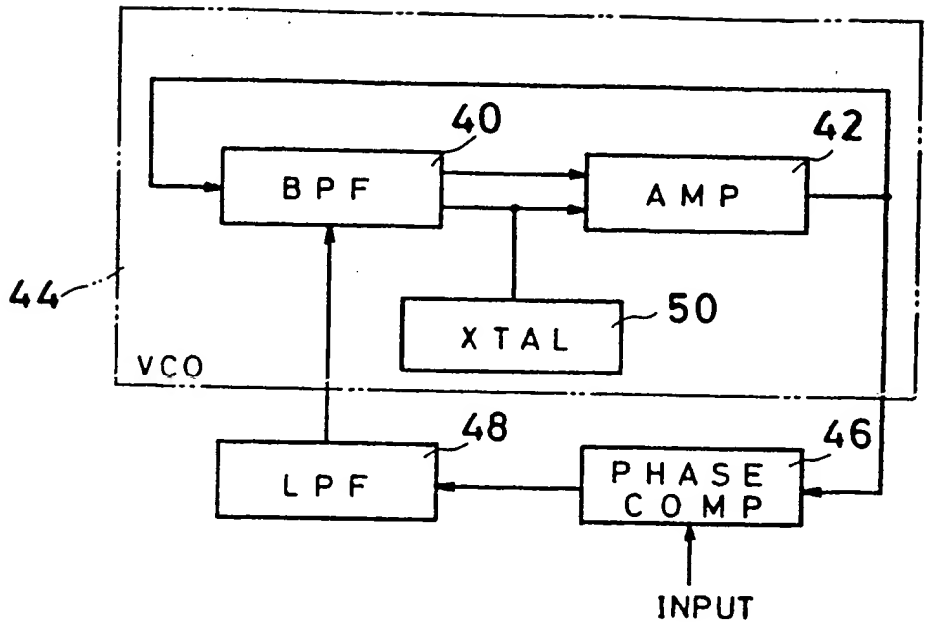

40
42
BPF
AMP
44
50
XTAL
VCO
48
46
LPF
PHASE COMP
INPUT

FIG.20

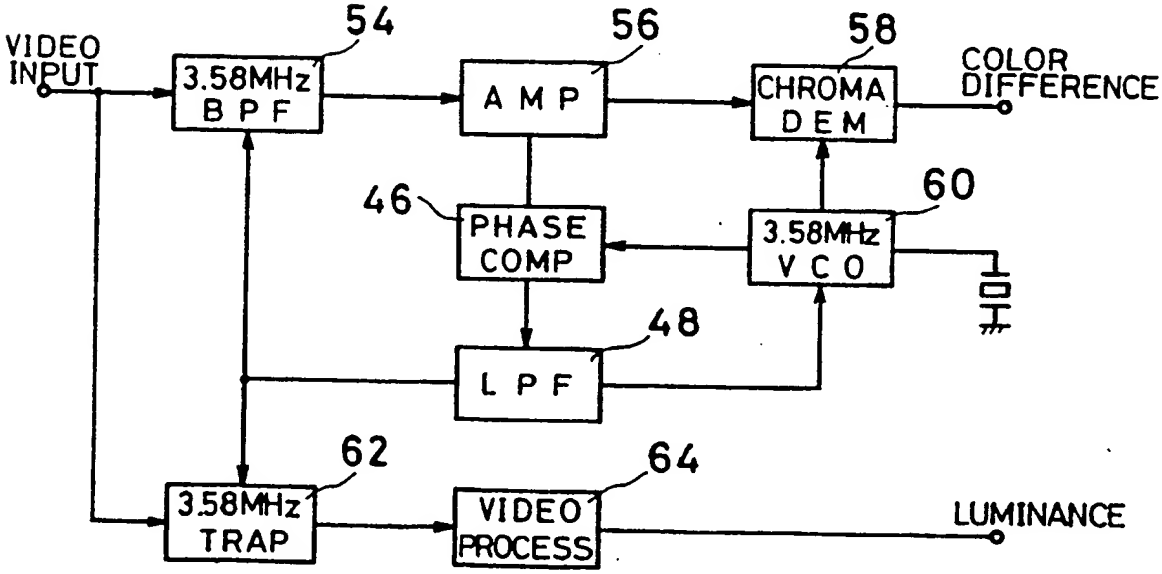

VIDEO INPUT
54
3.58MHz BPF
56
AMP
58
CHROMA DEM
COLOR DIFFERENCE
46
PHASE COMP
60
3.58MHz VCO
48
LPF
62
3.58MHz TRAP
64
VIDEO PROCESS
LUMINANCE

FIG. 21

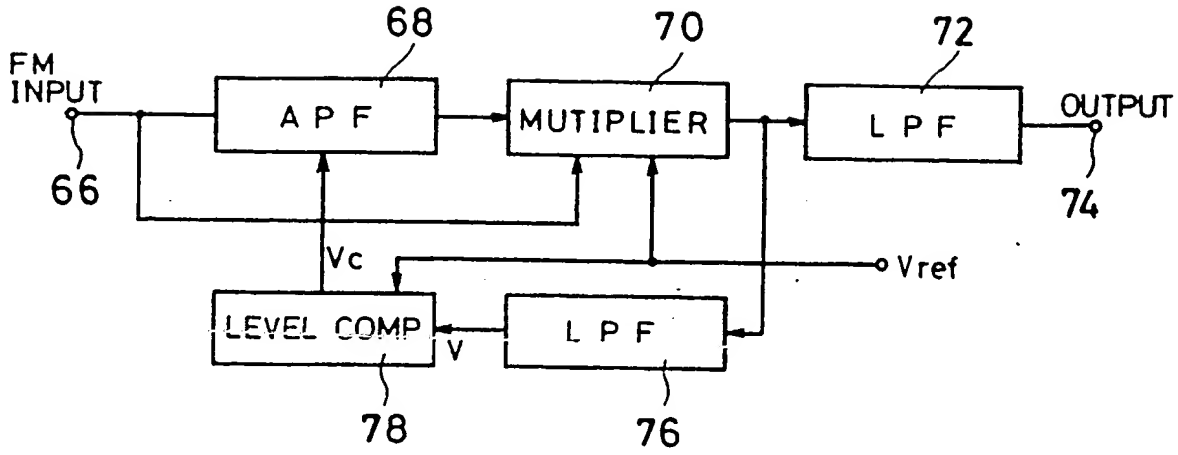

FM
INPUT
66
68
APF
70
MUTIPLIER
72
LPF
OUTPUT
74
Vc
Vref
LEVEL COMP
V
LPF
78
76

FIG. 22

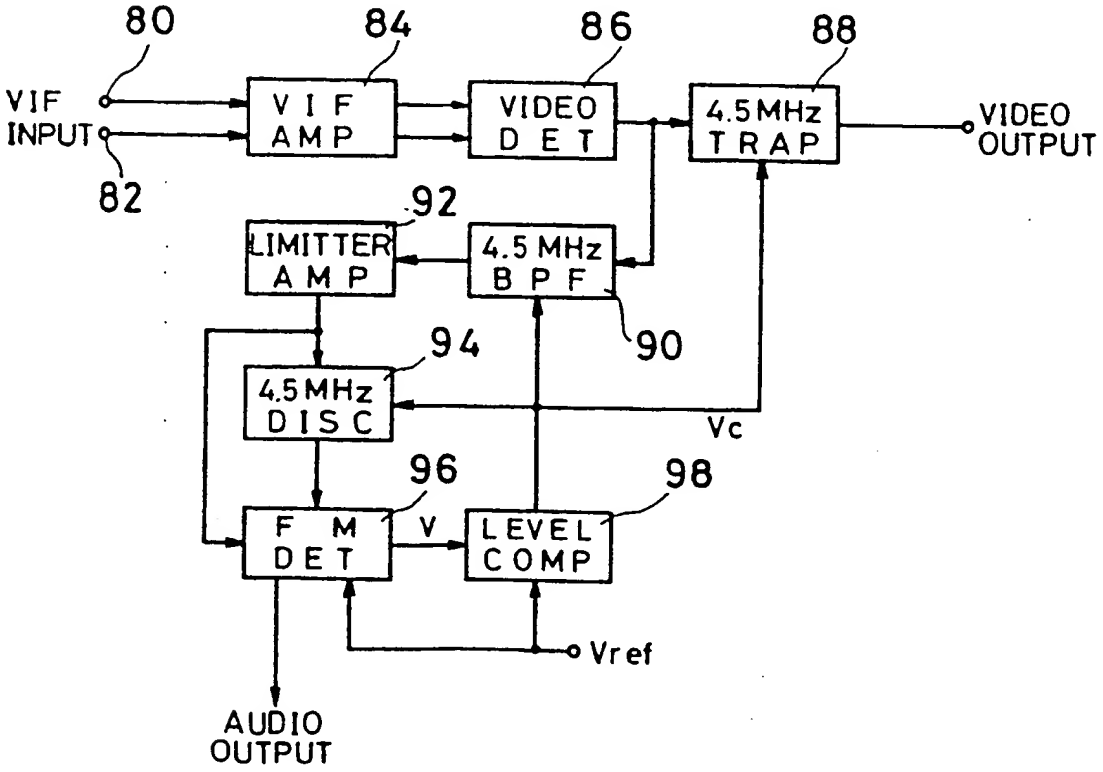
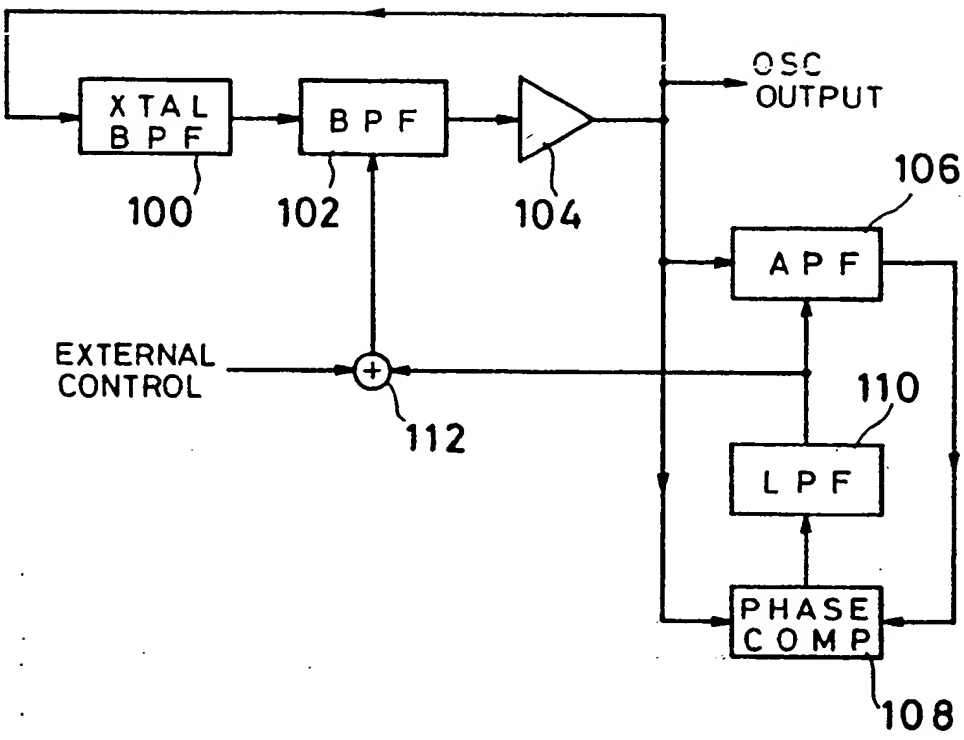

80
VIF
INPUT
82
84
VIF
AMP
86
VIDEO
DET
88
4.5MHz
TRAP
VIDEO
OUTPUT
92
LIMITTER
AMP
4.5 MHz
BPF
90
94
4.5MHz
DISC
Vc
96
98
FM
DET
V
LEVEL
COMP
Vref
AUDIO
OUTPUT

FIG. 23


XTAL BPF
BPF
OSC OUTPUT
100
102
104
106
APF
EXTERNAL CONTROL
110
112
LPF
PHASE COMP
108

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 393 717 A3**

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: 90107578.8

(51) Int. Cl.5 H03H 11/12

(22) Date of filing: 20.04.90

(30) Priority: 20.04.89 JP 100767/89
28.09.89 JP 252578/89
28.09.89 JP 252579/89

(43) Date of publication of application:
24.10.90 Bulletin 90/43

(84) Designated Contracting States:
DE ES FR GB IT

(88) Date of deferred publication of the search report:
19.06.91 Bulletin 91/25

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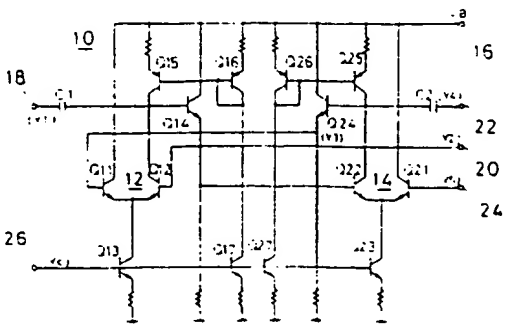
(54) **Active filter circuit.**

(57) An active filter circuit includes a first (10) and second (14) differential pairs each having a pair of transistors. A capacitor (C_1, C_2) is connected to a collector of each on transistor of the first and second differential pairs. A first and second negative feedback paths are connected, respectively, between the collector and a base of one transistor of the first differential pair and between the collector of one transistor of the second differential pair and a base of the other transistor of the first differential pair. By applying suitable voltages to respective inputs of the differential pairs, the active filter circuit functions as a band-pass filter, lowpass filter, high-pass filter, band elimination filter or phase-shifting filter with the same circuit configuration. A current source circuit (Q_{11}, Q_{12}) correlatively changes current amounts of the first and second differential pairs in response to a control voltage whereby a filter characteristic can be changed.

F I G. 4



EP 0 393 717 A3

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EUROPEAN SEARCH REPORT

Application Number

EP 90 10 7578

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	IEEE TRANSACTIONS ON CONSUMER ELECTRONICS, vol. CE-32, no. 3, August 1986, pages 644-650, New York, US; T. FUKUDA et al.: "A fully integrated filter circuit for VCRs" * Figures 5-9; page 646: "3-2. High-order filters" - page 648: "4-1. Emphasis characteristics" *	1-3	H 03 H 11 12
A	IDEM	10,11,13, 14	
X	EDN/EEE, vol. 17, no. 3, 1st February 1972, pages 38-41, Denver, US; G.J. DEBOO et al.: "Automatically tuned filter uses IC operational amplifiers" * The whole document *	1,12	
A	DE-A-3 803 179 (TOSHIBA) * The whole document *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 03 H

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
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E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document